DAQ

DAQCard™-6062E
User Manual

Multifunction I/O Device for PCMCIA

NATIONAL INSTRUMENTS™

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Worldwide Technical Support and Product Information

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FCC/Canada Radio Frequency Interference Compliance*

Determining FCC Class

The Federal Communications Commission (FCC) has rules to protect wireless communications from interference. The FCC places digital electronics into two classes. These classes are known as Class A (for use in industrial-commercial locations only) or Class B (for use in residential or commercial locations). Depending on where it is operated, this product could be subject to restrictions in the FCC rules. (In Canada, the Department of Communications (DOC), of Industry Canada, regulates wireless interference in much the same way.)

Digital electronics emit weak signals during normal operation that can affect radio, television, or other wireless products. By examining the product you purchased, you can determine the FCC Class and therefore which of the two FCC/DOC Warnings apply in the following sections. (Some products may not be labeled at all for FCC; if so, the reader should then assume these are Class A devices.)

FCC Class A products only display a simple warning statement of one paragraph in length regarding interference and undesired operation. Most of our products are FCC Class A. The FCC rules have restrictions regarding the locations where FCC Class A products can be operated.

FCC Class B products display either a FCC ID code, starting with the letters **EXN**, or the FCC Class B compliance mark that appears as shown here on the right.

Consult the FCC Web site at `www.fcc.gov` for more information.

FCC/DOC Warnings

This equipment generates and uses radio frequency energy and, if not installed and used in strict accordance with the instructions in this manual and the CE Mark Declaration of Conformity**, may cause interference to radio and television reception. Classification requirements are the same for the FCC and the Canadian DOC.

Changes or modifications not expressly approved by National Instruments could void the user's authority to operate the equipment under the FCC Rules.

Class A

Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Canadian Department of Communications

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe A respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

Class B

Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Canadian Department of Communications

This Class B digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe B respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

Compliance to EU Directives

Readers in the European Union (EU) must refer to the Manufacturer's Declaration of Conformity (DoC) for information** pertaining to the CE Mark compliance scheme. The Manufacturer includes a DoC for most every hardware product except for those bought for OEMs, if also available from an original manufacturer that also markets in the EU, or where compliance is not required as for electrically benign apparatus or cables.

To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by your product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.

* Certain exemptions may apply in the USA, see FCC Rules §15.103 **Exempted devices**, and §15.105(c). Also available in sections of CFR 47.

** The CE Mark Declaration of Conformity will contain important supplementary information and instructions for the user or installer.

Contents

Chapter 4
Signal Connections

About This Manual

This manual describes the electrical and mechanical aspects of the National Instruments DAQCard-6062E and contains information about operation and programming.

Conventions Used in This Manual

The following conventions are used in this manual.

< >
: Angle brackets containing numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, DIO<3..0>. Angle brackets can also denote a variable in a channel name—for example, ACH<*i*> and ACH<*i*+8>.

»
: The » symbol leads you through nested menu items and dialog box options to a final action. The sequence **File»Page Setup»Options** directs you to pull down the **File** menu, select the **Page Setup** item, and select **Options** from the last dialog box.


: This icon denotes a note, which alerts you to important information.


: This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash.When this symbol is marked on the product, refer to the *Safety Information* section of Chapter 1, *Introduction*, for precautions to take.

bold
: Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names.

italic
: Italic text denotes variables, emphasis, a cross reference, or an introduction to a key concept. This font also denotes text that is a placeholder for a word or value that you must supply.

`monospace`
: Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and code excerpts.

NI-DAQ
: NI-DAQ refers to NI-DAQ software unless otherwise noted.

Related Documentation

The following documents contain useful information related to the DAQCard-6062E:

- *DAQ Quick Start Guide*, located at `ni.com/manuals`
- *DAQ-STC Technical Reference Manual*, located at `ni.com/manuals`
- *NI-DAQ Function Reference Help*, accessible by selecting **Start» Programs»National Instruments»NI-DAQ»NI-DAQ Help**
- *NI-DAQ User Manual for PC Compatibles*, located at `ni.com/manuals`
- The NI Developer Zone tutorial, *Field Wiring and Noise Consideration for Analog Signals*, located at `ni.com/zone`

1

Introduction

This chapter describes the DAQCard-6062E, lists what you need to get started, explains how to unpack the DAQCard-6062E, and describes the optional software and equipment.

About the DAQCard-6062E

Thank you for buying a DAQCard-6062E. The DAQCard-6062E is a multifunction analog, digital, and timing I/O data acquisition (DAQ) device for computers equipped with Type II PCMCIA slots. This device features a 12-bit A/D converter (ADC), two 12-bit D/A converters (DACs), eight lines of TTL-compatible digital I/O (DIO), and two 24-bit counter/timers for timing I/O (TIO).

The DAQCard-6062E uses the National Instruments DAQ-STC system timing controller for time-related functions. The DAQ-STC consists of three timing groups that control analog input (AI), analog output (AO), and general-purpose counter/timer functions. These groups include a total of seven 24-bit and three 16-bit counters and have a maximum timing resolution of 50 ns.

The DAQCard-6062E can interface to an SCXI system so that you can acquire over 3,000 analog signals from thermocouples, resistance temperature detectors (RTDs), strain gauges, voltage sources, and current sources. You can also acquire or generate digital signals for communication and control. SCXI is the instrumentation front end for plug-in DAQ devices.

Detailed specifications for the DAQCard-6062E are in Appendix A, *Specifications*.

What You Need to Get Started

To set up and use the DAQCard-6062E, you need the following:

- ❑ The DAQCard-6062E
- ❑ *DAQCard-6062E User Manual*
- ❑ NI-DAQ for PC Compatibles
- ❑ Optional: One of the following software packages and documentation:
  - LabVIEW (Windows)
  - Measurement Studio (Windows)
  - VI Logger (Windows)
- ❑ A computer

Software Programming Choices

When programming the National Instruments DAQ hardware, you can use NI application development environment (ADE) software or other ADEs. In either case, use NI-DAQ.

NI-DAQ

NI-DAQ, which ships with the device, has an extensive library of functions that you can call from your ADE. These functions allow you to use all of the features of the device.

NI-DAQ carries out many of the complex interactions, such as programming interrupts, between the computer and the DAQ hardware. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to your code. Whether you are using LabVIEW, Measurement Studio, VI Logger, or other ADEs, your application uses NI-DAQ, as illustrated in Figure 1-1.

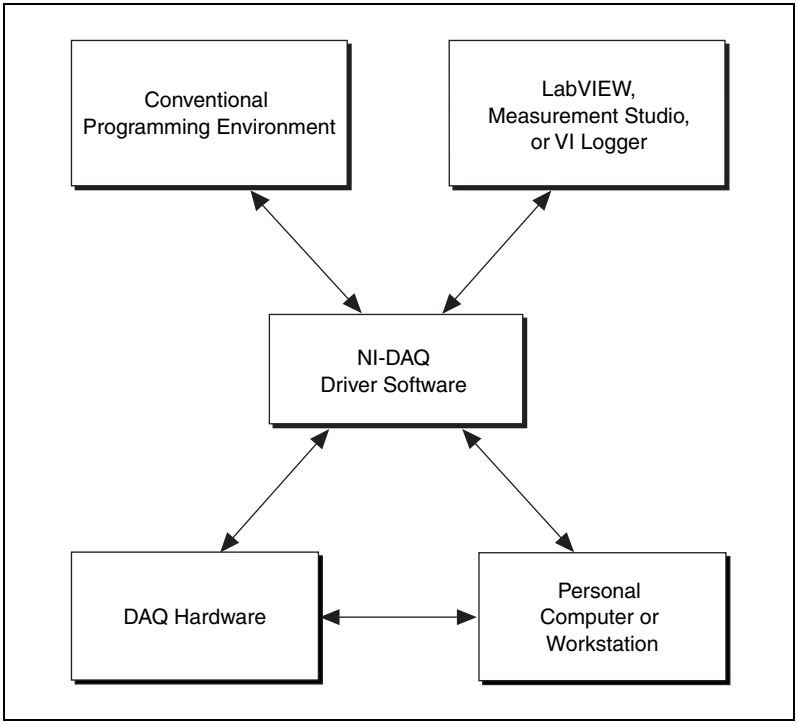


Figure 1-1. The Relationship Among the Programming Environment, NI-DAQ, and Your Hardware

To download a free copy of the most recent version of NI-DAQ, click **Download Software** at `ni.com`.

National Instruments ADE Software

LabVIEW features interactive graphics, a state-of-the-art interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of virtual instruments for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW.

Measurement Studio, which includes LabWindows/CVI, tools for Visual C++, and tools for Visual Basic, is a development suite that allows you to use ANSI C, Visual C++, and Visual Basic to design your test and measurement software. For C developers, Measurement Studio includes LabWindows/CVI, a fully integrated ANSI C application development environment that features interactive graphics and the LabWindows/CVI Data Acquisition and Easy I/O libraries. For Visual Basic developers, Measurement Studio features a set of ActiveX controls for using National

Instruments DAQ hardware. These ActiveX controls provide a high-level programming interface for building virtual instruments. For Visual C++ developers, Measurement Studio offers a set of Visual C++ classes and tools to integrate those classes into Visual C++ applications. The libraries, ActiveX controls, and classes are available with Measurement Studio and NI-DAQ.

VI Logger is an easy-to-use yet flexible tool specifically designed for data logging applications. Using dialog windows, you can configure data logging tasks to easily acquire, log, view, and share your data. VI Logger does not require any programming; it is a stand-alone, configuration-based software.

Using LabVIEW, Measurement Studio, or VI Logger greatly reduces the development time for your data acquisition and control application.

Optional Equipment

National Instruments offers a variety of products to use with the DAQCard-6062E, including the following cables, connector blocks, and other accessories:

- Cables and cable assemblies, shielded and ribbon
- Connector blocks, shielded and unshielded, with 50- and 68-pin screw terminals
- SCXI modules and accessories for isolating, amplifying, exciting, and multiplexing signals for relays and analog output. With SCXI, you can condition and acquire up to 3,072 channels.
- Low channel-count signal conditioning modules, cards, and accessories, including conditioning for strain gauges and RTDs, simultaneous sample-and-hold circuitry, and relays.

For more specific information about these products, refer to the NI catalog at `ni.com/catalog`.

Custom Cabling

National Instruments offers cables and accessories for you to prototype your application or to use if you frequently change DAQCard-6062E interconnections.

If you want to develop your own cable, however, the following guidelines may be useful:

- For the AI signals, shielded twisted-pair wires for each AI pair yield the best results, assuming that you use differential inputs. Tie the shield for each signal pair to the ground reference at the source.
- You should route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

National Instruments recommends the SHC68-68-EP cable. The SHC68-68-EP cable is a shielded, latching 68-pin cable that mates to the DAQCard I/O connector. This cable connects to the DAQCard 68-position VHDCI connector on one end and terminates with a 68-pin 0.050 series D-type connector on the other end.

Unpacking

The DAQCard-6062E is shipped in an antistatic package to prevent electrostatic damage to the device. Electrostatic discharge can damage several components on the device.

Caution *Never* touch the exposed pins of connectors.

To avoid such damage in handling the device, take the following precautions:

- Ground yourself using a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of the computer chassis before removing the device from the package.

Remove the DAQCard-6062E from the package and inspect the device for loose components or any sign of damage. Notify NI if the device appears damaged in any way. Do not install a damaged device into the computer.

Store the DAQCard-6062E in the antistatic package when not in use.

Safety Information

The following section contains important safety information that you *must* follow when installing and using the product.

Do *not* operate the product in a manner not specified in this document. Misuse of the product can result in a hazard. You can compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to National Instruments for repair.

Do *not* substitute parts or modify the product except as described in this document. Use the product only with the chassis, modules, accessories, and cables specified in the installation instructions. You *must* have all covers and filler panels installed during operation of the product.

Do *not* operate the product in an explosive atmosphere or where there may be flammable gases or fumes. Operate the product only at or below the pollution degree stated in Appendix A, *Specifications*. Pollution is foreign matter in a solid, liquid, or gaseous state that can reduce dielectric strength or surface resistivity. The following is a description of pollution degrees:

- Pollution degree 1 means no pollution or only dry, nonconductive pollution occurs. The pollution has no influence.
- Pollution degree 2 means that only nonconductive pollution occurs in most cases. Occasionally, however, a temporary conductivity caused by condensation must be expected.
- Pollution degree 3 means that conductive pollution occurs, or dry, nonconductive pollution occurs that becomes conductive due to condensation.

Clean the product with a soft nonmetallic brush. Make sure that the product is completely dry and free from contaminants before returning it to service.

You *must* insulate signal connections for the maximum voltage for which the product is rated. Do *not* exceed the maximum ratings for the product. Remove power from signal lines before connecting them to or disconnecting them from the product.

Operate this product only at or below the installation category stated in Appendix A, *Specifications*.

The following is a description of installation categories:

- Installation Category I is for measurements performed on circuits not directly connected to MAINS[1]. This category is a signal level such as voltages on a printed wire board (PWB) on the secondary of an isolation transformer.

  Examples of Installation Category I are measurements on circuits not derived from MAINS and specially protected (internal) MAINS-derived circuits.

- Installation Category II is for measurements performed on circuits directly connected to the low-voltage installation. This category refers to local-level distribution such as that provided by a standard wall outlet.

  Examples of Installation Category II are measurements on household appliances, portable tools, and similar equipment.

- Installation Category III is for measurements performed in the building installation. This category is a distribution level referring to hardwired equipment that does not rely on standard building insulation.

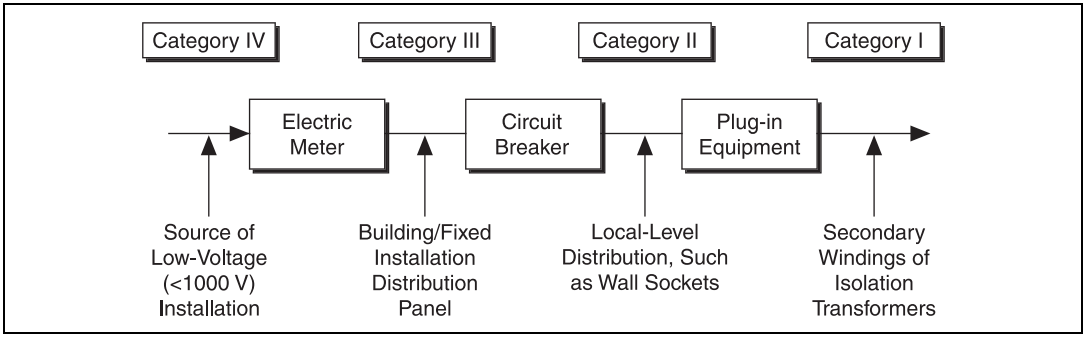
  Examples of Installation Category III include measurements on distribution circuits and circuit breakers. Other examples of Installation Category III are wiring including cables, bus-bars, junction boxes, switches, socket outlets in the building/fixed installation, and equipment for industrial use, such as stationary motors with a permanent connection to the building/fixed installation.

- Installation Category IV is for measurements performed at the source of the low-voltage (<1,000 V) installation.

  Examples of Installation Category IV are electric meters, and measurements on primary overcurrent protection devices and ripple-control units.

[1] MAINS is defined as the electricity supply system to which the equipment concerned is designed to be connected either for powering the equipment or for measurement purposes.

Below is a diagram of a sample installation.



2

Installing and Configuring the DAQCard-6062E

This chapter explains how to install and configure a DAQCard-6062E.

Installing the Software

Complete the following steps to install the software before installing the DAQCard-6062E.

1. Install the ADE, such as LabVIEW, Measurement Studio, or VI Logger, according to the instructions on the CD and the release notes.
2. Install NI-DAQ according to the instructions on the CD and the *DAQ Quick Start Guide* included with the device.

Note It is important to install NI-DAQ before installing the DAQCard-6062E to ensure that the device is properly detected.

Installing the Hardware

The following are general installation instructions. Consult the computer user manual or technical reference manual for specific instructions and warnings about installing new devices. Refer to Figure 2-1 when installing the DAQCard-6062E.

1. Power off and unplug the computer.
2. Insert the PCMCIA bus connector of the DAQCard-6062E in any available Type II PC Card slot until the connector is firmly seated. The DAQCard-6062E has two connectors—a 68-pin PCMCIA bus connector on one end and a 68-pin I/O connector on the other end. The DAQCard-6062E and the I/O cable are keyed so that you can only insert it one way.
3. Visually verify the installation by making sure that the DAQCard-6062E is fully inserted into the slot.

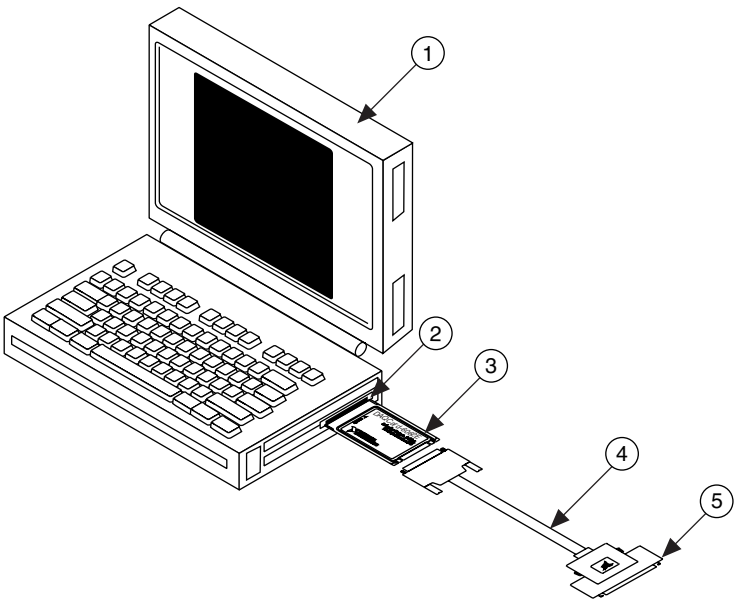
4. Attach the I/O cable. You can connect the DAQCard-6062E to 68- and 50-pin accessories. You can use the SHC68-68-EP to connect directly to 68-pin accessories, or you can use the SHC68-68-EP in conjunction with the 68M-50F adapter to connect to 50-pin accessories. Refer to Appendix B, *Optional Cable Connector Descriptions*, for more information.

Note Be careful not to put strain on the I/O cable when inserting it into and removing it from the DAQCard-6062E. Always grasp the cable by the connector you are plugging or unplugging. *Never* pull directly on the I/O cable to unplug it from the DAQCard-6062E.

5. Plug in and power on the computer.

The DAQCard-6062E is now installed. You are ready to make the appropriate connections to the I/O connector cable as described in Chapter 4, *Signal Connections*.

Figure 2-1 shows an example of a typical configuration.



1	Portable Computer	3	DAQCard-6062E	5	I/O Signals
2	PCMCIA Socket	4	SHC68-68-EP		

Figure 2-1. A Typical Configuration for the DAQCard-6062E

Configuring the Hardware

Because of the NI standard architecture for data acquisition, the DAQCard-6062E is completely software configurable.

Data acquisition-related configuration, which you must perform, includes such settings as AI coupling and range, and others. You can modify these settings using NI-DAQ or application-level software, such as LabVIEW and Measurement Studio.

To configure the device in Measurement & Automation Explorer (MAX), refer to the *DAQ Quick Start Guide* or to the *NI-DAQ User Manual for PC Compatibles*.

3

Hardware Overview

This chapter presents an overview of the hardware functions on the DAQCard-6062E.

Figure 3-1 shows the block diagram for the DAQCard-6062E.

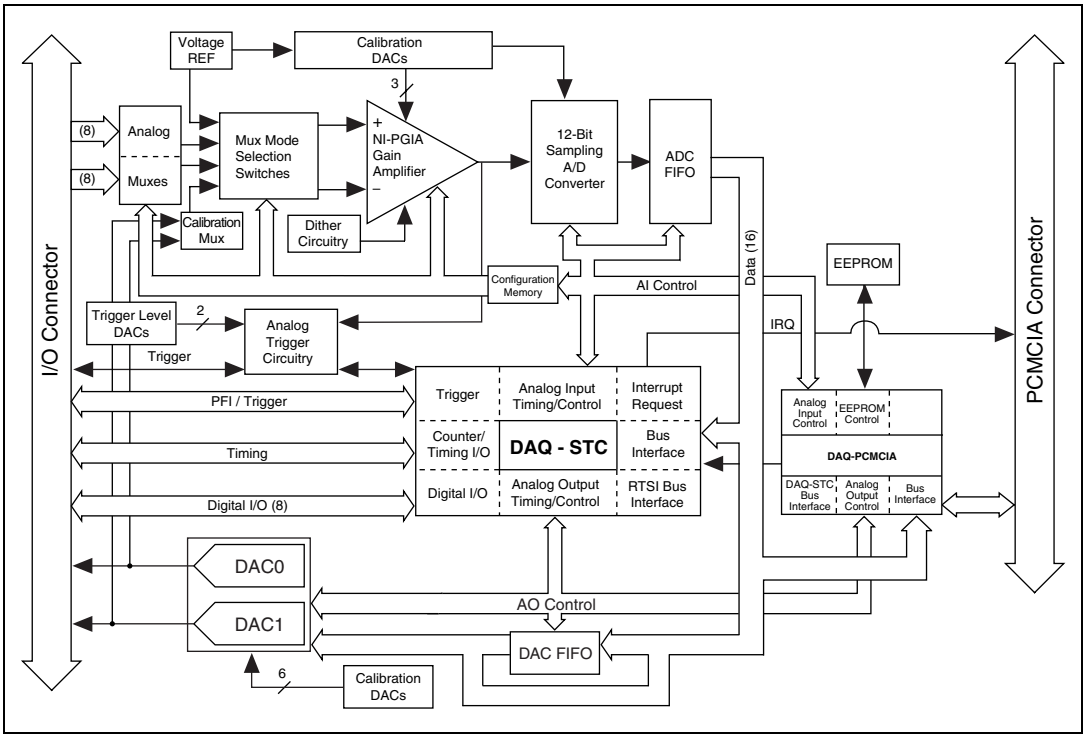


Figure 3-1. DAQCard-6062E Block Diagram

Analog Input

The AI section of the DAQCard-6062E is software configurable. You can select different AI configurations through application software designed to control the DAQCard-6062E. The following sections describe in detail each AI category.

Input Mode

The DAQCard-6062E has three input modes: nonreferenced single-ended (NRSE) input, referenced single-ended (RSE) input, and differential (DIFF) input. The single-ended input configurations use up to 16 channels. The DIFF input configuration uses up to eight channels. Input modes are programmed on a per channel basis for multimode scanning. For example, you can configure the circuitry to scan 12 channels—four differentially configured channels and eight single-ended channels. Table 3-1 describes the three input modes.

Table 3-1. Available Input Modes for the DAQCard-6062E

Configuration	Description
DIFF	A channel configured in DIFF mode uses two analog channel input lines. One line connects to the positive input of the DAQCard-6062E programmable gain instrumentation amplifier (PGIA), and the other connects to the negative input of the PGIA.
RSE	A channel configured in RSE mode uses one analog channel input line, which connects to the positive input of the PGIA. The negative input of the PGIA is internally connected to AI ground (AIGND).
NRSE	A channel configured in NRSE mode uses one analog channel input line, which connects to the positive input of the PGIA. The negative input of the PGIA connects to the AI sense (AISENSE) input.

For more information about the three input modes, refer to the *Analog Input Signal Connections* section of Chapter 4, *Signal Connections*, which contains diagrams showing the signal paths for the three configurations.

Input Polarity and Input Range

The DAQCard-6062E has two input polarities: unipolar and bipolar. Unipolar input polarity means that the input voltage range is between 0 and V_{ref}, where V_{ref} is a positive reference voltage. Bipolar input polarity means that the input voltage range is between $-V_{ref}/2$ and $+V_{ref}/2$. The DAQCard-6062E has a unipolar input range of 10 V (0 to 10 V) and a bipolar input range of 10 V (±5 V). You can program polarity and range settings on a per channel basis so that you can uniquely configure each input channel.

The software-programmable gain on these cards increases their overall flexibility by matching the input signal ranges to those that the ADC can accommodate. The DAQCard-6062E has gains of 0.5, 1, 2, 5, 10, 20, 50, and 100 and is suited for a wide variety of signal levels. With the proper gain setting, you can use the full resolution of the ADE to measure the input signal. Table 3-2 shows the overall input range and precision according to the range configuration and gain used.

Table 3-2. Actual Range and Measurement Precision

Range Configuration	Gain	Actual Input Range	Resolution[1]
0 to +10 V	1.0	0 to +10 V	2.44 mV
	2.0	0 to +5 V	1.22 mV
	5.0	0 to +2 V	488.28 µV
	10.0	0 to +1 V	244.14 µV
	20.0	0 to +500 mV	122.07 µV
	50.0	0 to +200 mV	48.83 µV
	100.0	0 to +100 mV	24.41 µV
–5 to +5 V	0.5	–10 to +10 V	4.88 mV
	1.0	–5 to +5 V	2.44 mV
	2.0	–2.5 to +2.5 V	1.22 mV
	5.0	–1 to +1 V	488.28 µV
	10.0	–500 to +500 mV	244.14 µV
	20.0	–250 to +250 mV	122.07 µV
	50.0	–100 to +100 mV	48.83 µV
	100.0	–50 to +50 mV	24.41 µV

[1] The value of 1 least significant bit (LSB) of the 12-bit ADC; that is, the voltage increment corresponding to a change of one count in the ADC 12-bit count.

Note: Refer to Appendix A, *Specifications*, for absolute maximum ratings.

Considerations for Selecting Input Ranges

Which input polarity and range you select depends on the expected range of the incoming signal. A large input range can accommodate a large signal variation but reduces the voltage resolution. Choosing a smaller input range improves the voltage resolution but may result in the input signal going out of range. For best results, you should match the input range as closely as possible to the expected range of the input signal. For example, if you are certain the input signal will not be negative (below 0 V), unipolar input polarity is best. However, if the signal is negative or equal to zero, inaccurate readings will occur if you use unipolar input polarity.

Dither

When you enable dither, you add approximately 0.5 LSB_{rms} of white Gaussian noise to the signal to be converted by the ADC. This addition is useful for applications involving averaging to increase the resolution of the DAQCard-6062E, such as calibration or spectral analysis. In such applications, noise modulation is decreased and differential linearity is improved by adding dither. When taking DC measurements, such as when checking the DAQCard-6062E calibration, you should enable dither and average about 1,000 points to take a single reading. This process removes the effects of quantization and reduces measurement noise, resulting in improved resolution. For high-speed applications not involving averaging or spectral analysis, you may want to disable the dither to reduce noise. You enable and disable the dither circuitry through software.

Figure 3-2 illustrates the effect of dither on signal acquisition. Figure 3-2a shows a small (±4 LSB) sine wave acquired with dither off. The quantization of the ADC is clearly visible. Figure 3-2b shows what happens when 50 such acquisitions are averaged together; quantization is still plainly visible. In Figure 3-2c, the sine wave is acquired with dither on. A considerable amount of noise is visible, but averaging about 50 such acquisitions, as shown in Figure 3-2d, eliminates both the added noise and the effects of quantization. Dither has the effect of forcing quantization noise to become a zero-mean random variable rather than a deterministic function of the input signal.

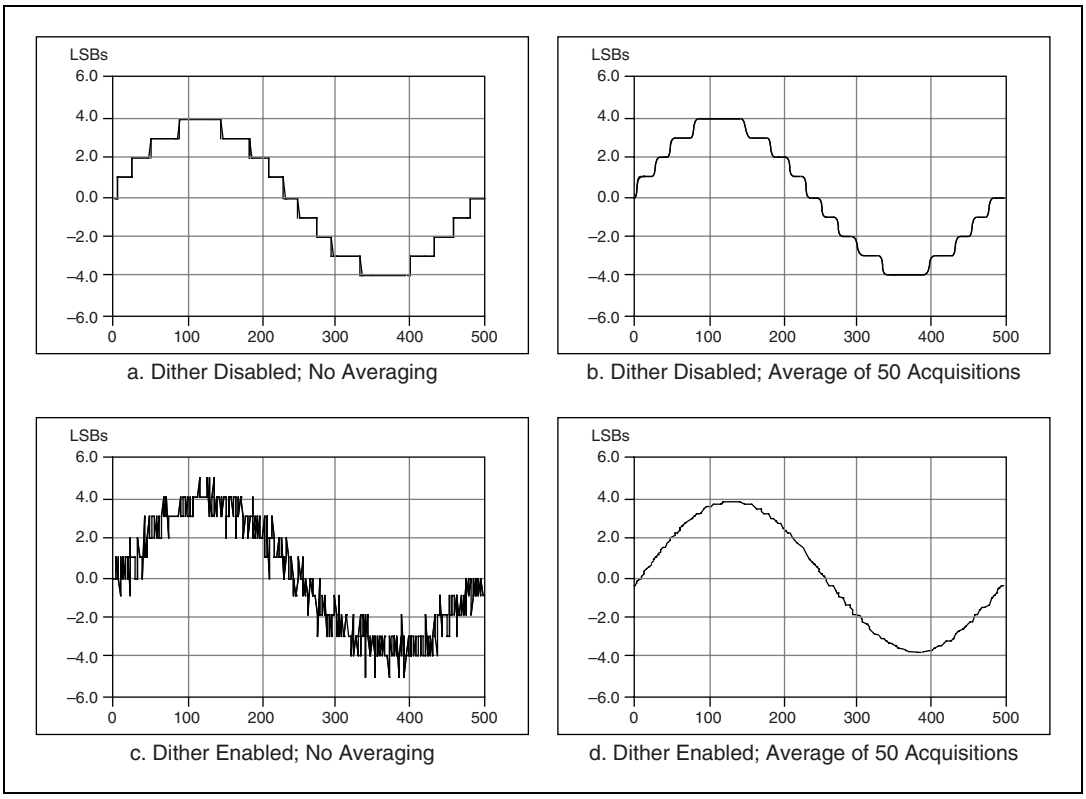


Figure 3-2. Dither

Multiple Channel Scanning Considerations

The DAQCard-6062E can scan multiple channels at the same maximum rate as the single-channel rate; however, notice the settling times. No extra settling time is necessary between channels as long as the gain is constant and source impedances are low. Refer to Appendix A, *Specifications*, for a complete listing of settling times.

Settling times can increase when scanning channels with various gains. When the PGIA switches to a higher gain, the signal on the previous channel may be well outside the new, smaller range. For instance, suppose a 4 V signal is connected to channel 0 and a 1 mV signal is connected to channel 1, and suppose the PGIA is programmed to apply a gain of one to channel 0 and a gain of 100 to channel 1. When the multiplexer switches to channel 1 and the PGIA switches to a gain of 100, the new full-scale range is 100 mV if the ADC is in unipolar mode. The approximately 4 V step from 4 V to 1 mV is 4,000% of the new full-scale range. The circuitry

can take as long as 100 µs to settle to 1 LSB after such a large transition. In general, this extra settling time is not needed when the PGIA switches to a lower gain.

A phenomenon called *charge injection*, in which the AI multiplexer injects a small amount of charge into each signal source when that source is selected, can cause settling times to increase when scanning high-impedance signals. If the impedance of the source is too high, the effect of the charge—a voltage error—has not decayed by the time the ADC samples the signal. For this reason, keep source impedances under 1 kΩ to perform high-speed scanning.

Multiple-channel scanning is not recommended unless sampling rates are low or you must sample several signals almost simultaneously. The data is more accurate and channel-to-channel independent if you independently acquire data from each channel (for example, 100 points from channel 0, then 100 points from channel 1, then 100 points from channel 2, and so on).

Analog Output

The DAQCard-6062E supplies two channels of AO voltage at the I/O connector. You can select the reference and the range for the AO circuitry using software. The reference can be either internal or external, and the range is bipolar only.

Analog Output Reference Selection

You can connect each DAC to the DAQCard-6062E internal reference of 10 V or to the external reference signal connected to the external reference (EXTREF) pin on the I/O connector. This signal applied to EXTREF should be between –11 and +11 V. You do not need to configure both channels for the same mode.

Analog Output Reglitch Selection

In normal operation, a DAC glitches whenever it is updated with a new value. The glitch energy differs from code to code and appears as distortion in the frequency spectrum. Each analog output of the DAQCard-6062E contains a reglitch circuit that generates uniform glitch energy at every code, rather than large glitches at the major code transitions. The uniform glitch energy appears as a multiple of the update rate in the frequency spectrum. Notice that this reglitch circuit does *not* elimiate the glitches; it only makes the more uniform in size. Reglitching is normally disabled at startup and can be independently enabled for each channel using software.

Analog Trigger

In addition to supporting internal software triggering and external digital triggering to initiate a DAQ sequence, the DAQCard-6062E also supports analog triggering. You can configure the analog trigger circuitry to accept either a direct analog input from the PFI0/TRIG1 pin on the I/O connector or a postgain signal from the output of the PGIA, as shown in Figure 3-3.

The trigger-level range for the direct analog channel is ±10 V in 78 mV steps. The range for the post-PGIA trigger selection is simply the full-scale range of the selected channel, and the resolution is that range divided by 256.

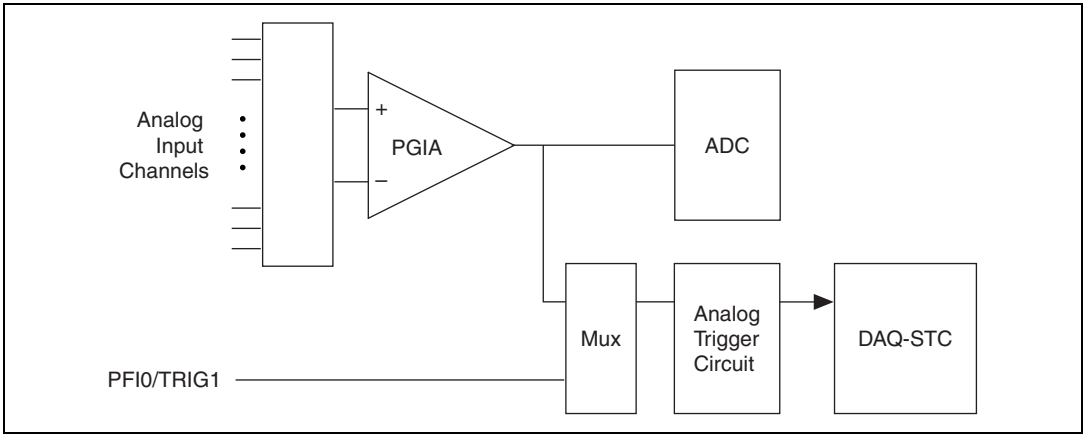


Figure 3-3. Analog Trigger Block Diagram

Five analog triggering modes are available, as shown in Figures 3-4 through 3-8. You can set **lowValue** and **highValue** independently in software.

In below-low-level analog triggering mode, as shown in Figure 3-4, the trigger is generated when the signal value is less than **lowValue**. **HighValue** is unused.

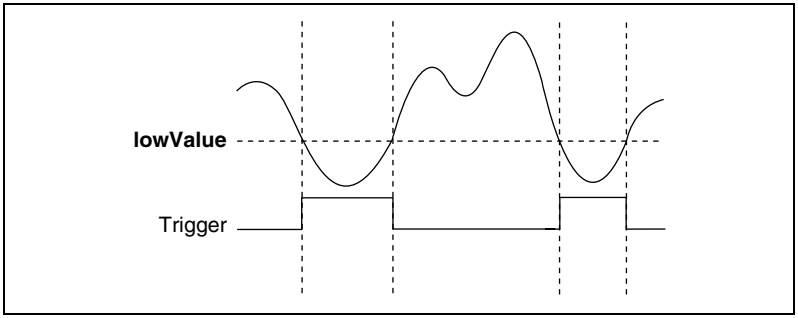


Figure 3-4. Below-Low-Level Analog Triggering Mode

In above-high-level analog triggering mode, as shown in Figure 3-5, the trigger is generated when the signal value is greater than **highValue**. **LowValue** is unused.

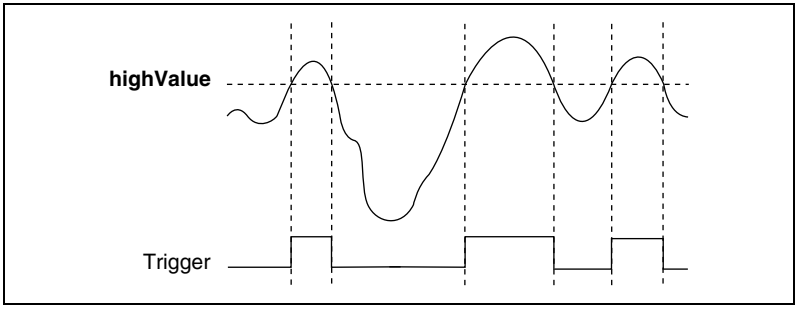


Figure 3-5. Above-High-Level Analog Triggering Mode

In inside-region analog triggering mode, as shown in Figure 3-6, the trigger is generated when the signal value is between the **lowValue** and the **highValue**.

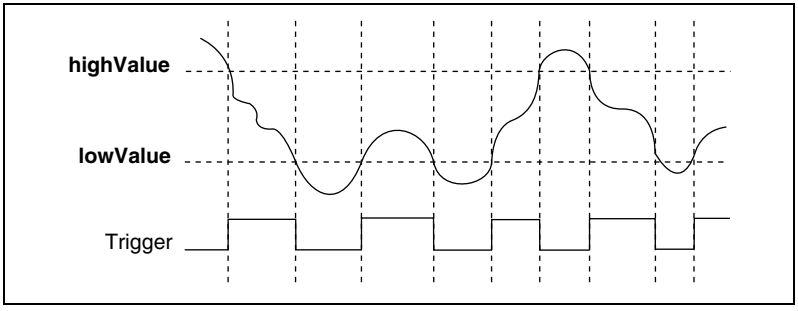


Figure 3-6. Inside-Region Analog Triggering Mode

In high-hysteresis analog triggering mode, as shown in Figure 3-7, the trigger is generated when the signal value is greater than **highValue**, with the hysteresis specified by **lowValue**.

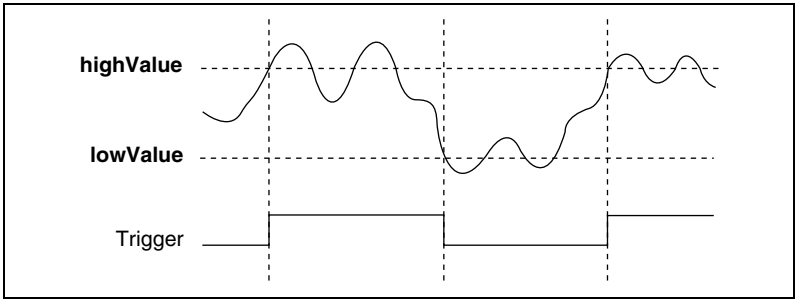


Figure 3-7. High-Hysteresis Analog Triggering Mode

In low-hysteresis analog triggering mode, as shown in Figure 3-8, the trigger is generated when the signal value is less than **lowValue**, with the hysteresis specified by **highValue**.

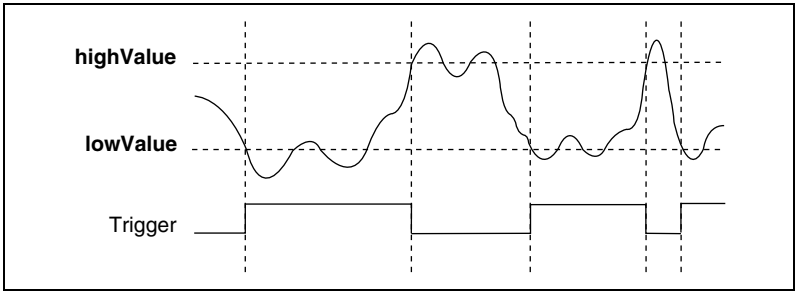


Figure 3-8. Low-Hysteresis Analog Triggering Mode

The analog trigger circuit generates an internal digital trigger based on the AI signal and the user-defined trigger levels. Any of the timing sections of the DAQ-STC, including the AI, AO, and general-purpose counter/timer sections, can use this digital trigger. For example, the AI section can be configured to acquire *n* scans after the AI signal crosses a specific threshold.

Digital I/O

The DAQCard-6062E contains eight lines of digital I/O for general-purpose use. You can individually configure each line through software for either input or output. At system startup and reset, the DIO ports are all high-impedance.

The hardware up/down control for general-purpose counters 0 and 1 are connected onboard to DIO6 and DIO7, respectively. Thus, you can use DIO6 and DIO7 to control the general-purpose counters. The up/down control signals, GPCTR0_UP_DOWN and GPCTR1_UP_DOWN, are input only and do not affect the operation of the DIO lines.

Timing Signal Routing

The DAQ-STC provides a flexible interface for connecting timing signals to other devices or external circuitry. The DAQCard-6062E uses the programmable function input (PFI) pins on the I/O connector to connect to external circuitry. These connections are designed to enable the DAQCard-6062E to both control and be controlled by other devices and circuits.

The DAQ-STC has 13 internal timing signals that can be controlled by an external source. These timing signals can also be controlled by signals generated internally to the DAQ-STC, and these selections are fully software configurable. For example, the signal routing multiplexer for controlling the CONVERT* signal is shown in Figure 3-9.

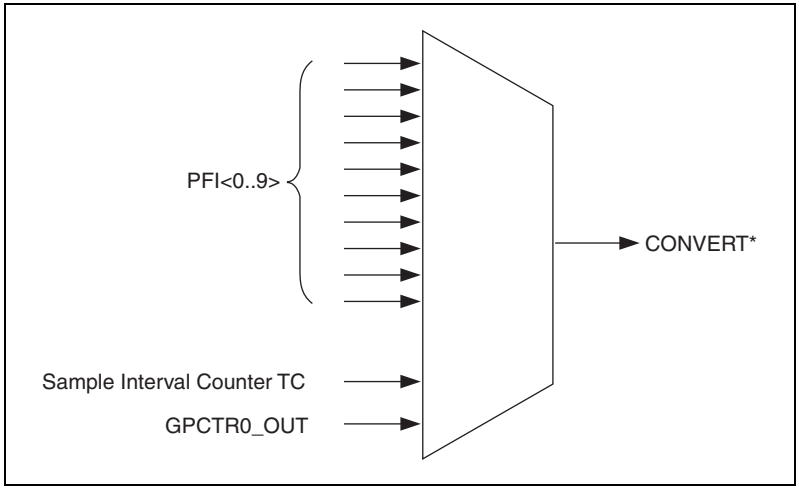


Figure 3-9. CONVERT* Signal Routing

Figure 3-9 shows that CONVERT* can be generated from a number of sources, including the external signals PFI<0..9> and the internal signals Sample Interval Counter TC and GPCTR0_OUT.

Programmable Function Inputs

Ten PFIs connect to the signal routing multiplexer for each timing signal, and software can select a PFI as the external source for a given timing signal. Any timing signal can use any PFI as an input, and multiple timing signals can simultaneously use the same PFI. This flexible routing scheme reduces the need to change physical connections to the I/O connector for different applications.

You also can individually enable each PFI pin to output a specific internal timing signal. For example, if you need the UPDATE* signal as an output on the I/O connector, software can turn on the output driver for the PFI5/UPDATE* pin.

DAQCard-6062E Clocks

Many functions performed by the DAQCard-6062E require a frequency timebase to generate the necessary timing signals for controlling A/D conversions, DAC updates, or general-purpose signals at the I/O connector.

The DAQCard-60602E can directly use the internal 20 MHz timebase as the primary frequency source.

4

Signal Connections

This chapter describes how to make input and output signal connections to the DAQCard-6062E through the DAQCard I/O connector.

Table 4-1 shows the cables that can be used with the I/O connectors to connect to different accessories.

Table 4-1. I/O Connector Details

Device with I/O Connector	Number of Pins	Cable for Connecting to 100-Pin Accessories	Cable for Connecting to 68-Pin Accessories	Cable for Connecting to 50-Pin Accessories
DAQCard-6062E	68	N/A	SHC68-68EP shielded cable RC68-68 ribbon cable	SHC68-68-EP with 68M-50F cable adapter

Caution Connections that exceed any of the maximum ratings of input or output signals on the devices can damage the device and the computer. Maximum input ratings for each signal are given in the *Protection* column of Table 4-3. NI is *not* liable for any damage resulting from such signal connections.

I/O Connector

Figure 4-1 shows the pin assignments for the 68-pin I/O connector on the DAQCard-6062E. A signal description follows the connector pinout.

Caution Exceeding the differential and common-mode input ranges distorts the input signals. Exceeding the maximum input voltage rating can damage the DAQCard-6062E and the computer. NI is *not* liable for any damage resulting from such signal connections. The maximum input voltage ratings are listed in the *Protection* column of Table 4-3.

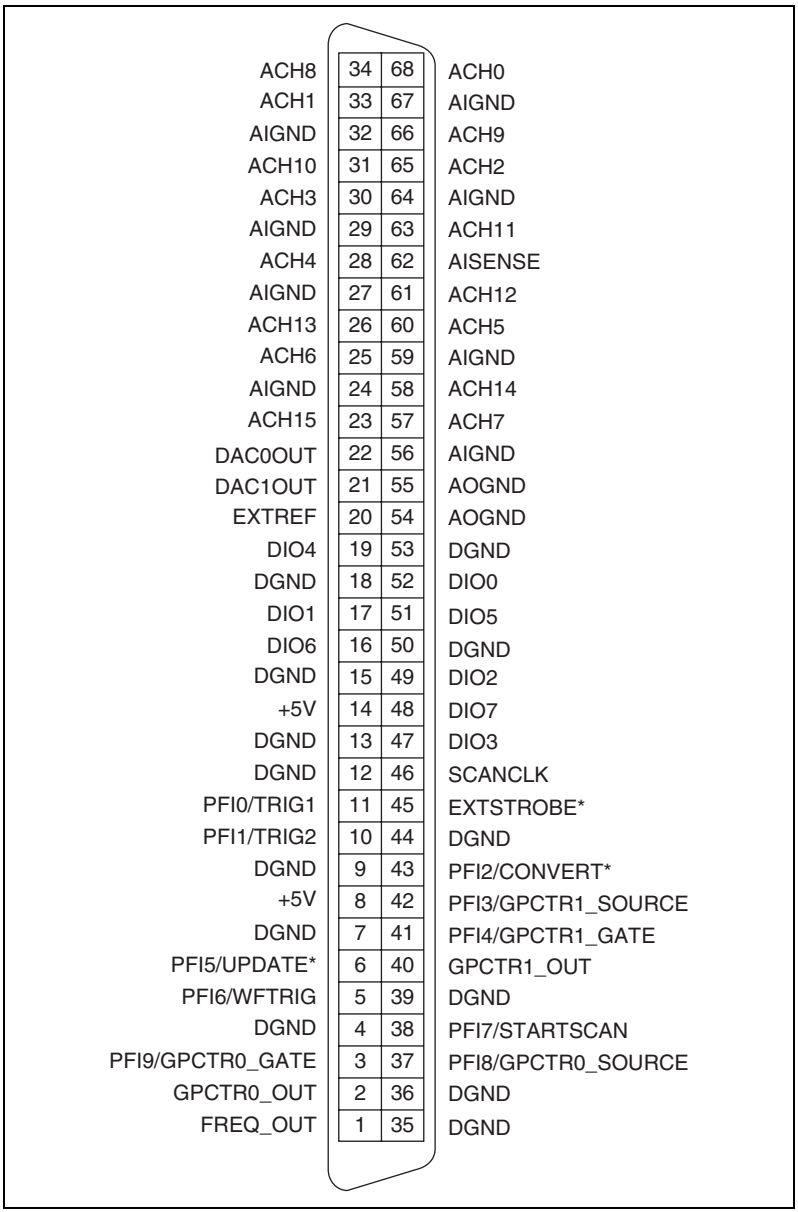


Figure 4-1. I/O Connector Pin Assignment for the DAQCard-6062E

Table 4-2 describes the DAQCard-6062E I/O connectors as diagrammed in Figure 4-1. Table 4-3 gives the I/O signal summary for these connections.

Table 4-2. I/O Connector Signal Descriptions

Signal Name	Reference	Direction	Description
AIGND	—	—	Analog Input Ground—These pins serve as the reference point for single-ended measurements and the bias current return point for differential measurements. All three ground references—AIGND, AOGND, and DGND—are connected on the DAQCard-6062E.
ACH<0..15>	AIGND	Input	Analog Input Channels 0 through 15—You can configure each channel pair, ACH<*i*, *i*+8> (*i* = 0..7), as either one differential input or two single-ended inputs.
AISENSE	AIGND	Input	Analog Input Sense—This pin serves as the reference node for any of channels ACH<0..15> in NRSE configuration.
DAC0OUT	AOGND	Output	Analog Channel 0 Output—This pin supplies the voltage output of AO channel 0.
DAC1OUT	AOGND	Output	Analog Channel 1 Output—This pin supplies the voltage output of AO channel 1.
AOGND	—	—	Analog Output Ground—This node references the AO voltages. All three ground references—AIGND, AOGND, and DGND—are connected on the DAQCard-6062E.
DGND	—	—	Digital Ground—This pin supplies the reference for the digital signals at the I/O connector as well as the +5 VDC supply. All three ground references—AIGND, AOGND, and DGND—are connected on the DAQCard-6062E.
DIO<0..7>	DGND	Input or Output	Digital I/O Signals—DIO6 and DIO7 can control the up/down signal of general-purpose counters 0 and 1, respectively.
+5V	DGND	Output	+5 VDC Source—These pins are fused for up to 250 mA of +5 V supply. The fuse is self-resetting.
SCANCLK	DGND	Output	Scan Clock—This pin pulses once for each A/D conversion in the scanning modes, when enabled. The low-to-high edge indicates when the input signal can be removed from the input or switched to another signal.
EXTSTROBE*	DGND	Output	External Strobe—This output can be toggled under software control to latch signals or trigger events on external devices.

Table 4-2. I/O Connector Signal Descriptions (Continued)

Signal Name	Reference	Direction	Description
PFI0/TRIG1	DGND	Input	PFI0/Trigger 1—As an input, this is a PFI or the source for the hardware analog trigger. PFI signals are explained in the *Connecting Timing Signals* section. The hardware analog trigger is explained in the *Analog Trigger* section of Chapter 3, *Hardware Overview*.
		Output	As an output, this is the TRIG1 (AI Start Trigger) signal. In posttriggered DAQ sequences, a low-to-high transition indicates the initiation of the acquisition sequence. In pretrigger applications, a low-to-high transition indicates the initiation of the pretrigger conversions.
PFI1/TRIG2	DGND	Input	PFI1/Trigger 2—As an input, this is a PFI.
		Output	As an output, this is the TRIG2 (AI Stop Trigger) signal. In pretrigger applications, a low-to-high transition indicates the initiation of the posttrigger conversions. TRIG2 is not used in posttrigger applications.
PFI2/CONVERT*	DGND	Input	PFI2/Convert—As an input, this is a PFI.
		Output	As an output, this is the CONVERT* (AI Convert) signal. A high-to-low edge on CONVERT* indicates that an A/D conversion is occurring.
PFI3/GPCTR1_SOURCE	DGND	Input	PFI3/Counter 1 Source—As an input, this is a PFI.
		Output	As an output, this is the GPCTR1_SOURCE signal. This signal reflects the actual source connected to general-purpose counter 1.
PFI4/GPCTR1_GATE	DGND	Input	PFI4/Counter 1 Gate—As an input, this is a PFI.
		Output	As an output, this is the GPCTR1_GATE signal. This signal reflects the actual gate signal connected to general-purpose counter 1.
GPCTR1_OUT	DGND	Output	Counter 1 Output—This output is from the general-purpose counter 1 output.
PFI5/UPDATE*	DGND	Input	PFI5/Update—As an input, this is a PFI.
		Output	As an output, this is the UPDATE* (AO Update) signal. A high-to-low edge on UPDATE* indicates that the AO primary group is being updated.
PFI6/WFTRIG	DGND	Input	PFI6/Waveform Trigger—As an input, this is a PFI.
		Output	As an output, this is the WFTRIG (AO Start Trigger) signal. In timed AO sequences, a low-to-high transition indicates the initiation of the waveform generation.

Table 4-2. I/O Connector Signal Descriptions (Continued)

Signal Name	Reference	Direction	Description
PFI7/STARTSCAN	DGND	Input Output	PFI7/Start of Scan—As an input, this is a PFI. As an output, this is the STARTSCAN (AI Scan Start) signal. This pin pulses once at the start of each AI scan in the interval scan. A low-to-high transition indicates the start of the scan.
PFI8/GPCTR0_SOURCE	DGND	Input Output	PFI8/Counter 0 Source—As an input, this is a PFI. As an output, this is the GPCTR0_SOURCE signal. This signal reflects the actual source connected to general-purpose counter 0.
PFI9/GPCTR0_GATE	DGND	Input Output	PFI9/Counter 0 Gate—As an input, this is a PFI. As an output, this is the GPCTR0_GATE signal. This signal reflects the actual gate signal connected to general-purpose counter 0.
GPCTR0_OUT	DGND	Output	Counter 0 Output—This output is from the general-purpose counter 0 output.
FREQ_OUT	DGND	Output	Frequency Output—This output is from the frequency generator output.

Table 4-3. I/O Signal Summary for the DAQCard-6062E

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
ACH<0..15>	AI	100 GΩ in parallel with 100 pF	25/10	—	—	—	±200 pA
AISENSE	AI	100 GΩ in parallel with 100 pF	25/10	—	—	—	±200 pA
AIGND	AI	—	—	—	—	—	—
DAC0OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	10 V/µs	—
DAC1OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	10 V/µs	—
AOGND	—	—	—	—	—	—	—
DGND	DO	—	—	—	—	—	—

Table 4-3. I/O Signal Summary for the DAQCard-6062E (Continued)

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
VCC	DO	0.45 Ω	Short-circuit to ground	250 at V_{cc}	—	—	—
DIO<0..7>	DIO	—	V_{cc} +0.5	13 at (V_{cc} –0.4)	24 at 0.4	1.1	50 kΩ pu[1]
SCANCLK	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
EXTSTROBE*	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI0/TRIG1	ADIO	10 kΩ	V_{cc} +0.5/±35	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu[2]
PFI1/TRIG2	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI2/CONVERT*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI3/GPCTR1_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI4/GPCTR1_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR1_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI5/UPDATE*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI6/WFTRIG	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI7/STARTSCAN	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI8/GPCTR0_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
PFI9/GPCTR0_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR0_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu

Table 4-3. I/O Signal Summary for the DAQCard-6062E (Continued)

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
FREQ_OUT	DO	—	—	3.5 at (V_{cc} –0.4)	5 at 0.4	1.5	50 kΩ pu

pu = pull up DO = Digital Output ADIO = Analog/Digital Input/Output

[1] DIO <6..7> are also pulled up with a 10 kΩ resistor.

[2] Also pulled down with a 10 kΩ resistor.

Note: The tolerance on the 50 kΩ pull-up and pull-down resistors is large; actual values may range between 17 kΩ and 100 kΩ.

Caution: Unless specifically indicated in the *Protection* column of Table 4-2, the outputs of DAQCard-6062E devices are not short-circuit protected. Exceeding the output limit in the *Source* and *Sink* columns can damage the DAQCard-6062E.

Analog Input Signal Connections

The AI signals are ACH<0..15>, AISENSE, and AIGND. The ACH<0..15> signals connect to the 16 AI channels of the DAQCard-6062E. In single-ended mode, signals connected to ACH<0..15> are routed to the positive input of the DAQCard PGIA. In DIFF mode, signals connected to ACH<0..7> are routed to the positive input of the PGIA, and signals connected to ACH<8..15> are routed to the negative input of the PGIA.

Caution Exceeding the differential and common-mode input ranges distorts the input signals[1]. Exceeding the maximum input voltage rating can damage the DAQCard-6062E and the computer. NI is *not* liable for any damage resulting from such signal connections. The maximum input voltage ratings are listed in the *Protection* column of Table 4-3.

In NRSE mode, the AISENSE signal internally connects to the negative input of the DAQCard PGIA when the corresponding channels are selected. In DIFF and RSE modes, this signal is unconnected.

AIGND is an AI common signal that is routed directly to the ground connection point on the DAQCard-6062E. You can use this signal for a general analog ground connect point to the device, if necessary.

Connection of AI signals to the DAQCard-6062E depends on the configuration of the AI channels you are using and the signal source type.

[1] Note that exceeding input ranges on any channel can affect the measurements on a different channel even if the other channel is well within the input range.

With the different configurations, you can use the PGIA in different ways. Figure 4-2 shows a diagram of the DAQCard PGIA.

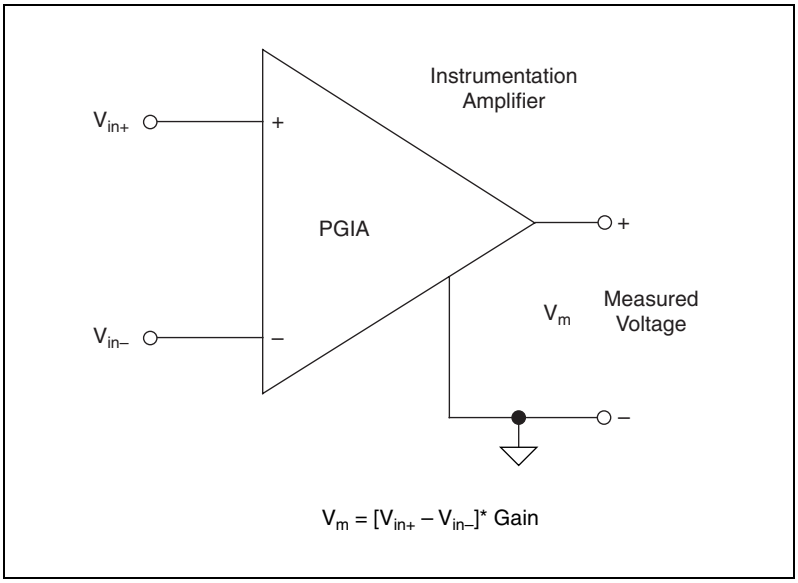


Figure 4-2. DAQCard-6062E PGIA

The PGIA applies gain and common-mode voltage rejection and presents high-input impedance to the AI signals connected to the DAQCard-6062E. Signals are routed to the positive and negative inputs of the PGIA through input multiplexers on the DAQCard-6062E. The PGIA converts two input signals to a signal that is the difference between the two input signals multiplied by the gain setting of the amplifier. The amplifier output voltage is referenced to the ground for the DAQCard-6062E. The DAQCard-6062E ADC measures this output voltage when it performs A/D conversions.

You must reference all signals to ground either at the source device or at the DAQCard-6062E. If you have a floating source, reference the signal to ground using RSE mode or the DIFF input configuration with bias resistors. Refer to the *Differential Connections for Nonreferenced or Floating Signal Sources* section for more information. If you have a grounded source, you should not reference the signal to AIGND. You can avoid this reference by using DIFF or NRSE input configurations.

Types of Signal Sources

When configuring the input channels and making signal connections, you must first determine whether the signal sources are floating or ground-referenced. The following sections describe these two signal types.

Floating Signal Sources

A floating signal source is one that is not connected in any way to the building ground system but, rather, has an isolated ground-reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolator output, and isolation amplifiers. An instrument or device that has an isolated output is a floating signal source. You must connect the ground reference of a floating signal to the DAQCard-6062E AI ground to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies as the source floats outside the common-mode input range.

Ground-Referenced Signal Sources

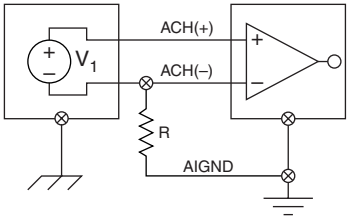
A ground-referenced signal source is one that is connected in some way to the building system ground and is, therefore, already connected to a common ground point with respect to the DAQCard-6062E, assuming that the computer is plugged into the same power system. Nonisolated output of instruments and devices that plug into the building power system falls into this category.

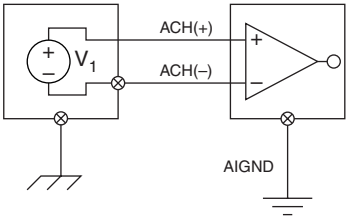
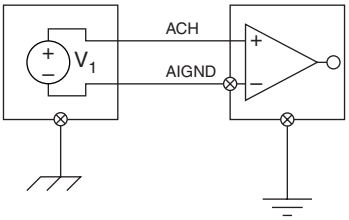
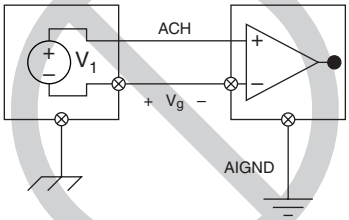
The difference in ground potential between two instruments connected to the same building power system is typically between 1 and 100 mV, but it can be much higher if power distribution circuits are improperly connected. If a grounded signal source is incorrectly measured, this difference may appear as a measurement error. The connection instructions for grounded signal sources are designed to eliminate this ground potential difference from the measured signal.

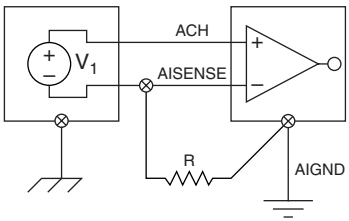
Input Configurations

You can configure the DAQCard-6062E for NRSE, RSE, or DIFF mode. The following sections discuss single-ended and differential measurements and considerations for measuring both types of signal sources.

Figure 4-3 summarizes the recommended input configuration for both types of signal sources.

<table>
<tr><th rowspan="2">Input</th><th colspan="2">Signal Source Type</th></tr>
<tr><th>Floating Signal Source
(Not Connected to Building Ground)</th><th>Grounded Signal Source</th></tr>
<tr><td></td><td>Examples
• Ungrounded Thermocouples
• Signal Conditioning with Isolated Outputs
• Battery Devices</td><td>Examples
• Plug-in Instruments with Nonisolated Outputs</td></tr>
<tr><td>Differential (DIFF)</td><td> 

See text for information on bias resistors.</td><td> 
</td></tr>
<tr><td>Single-Ended — Ground Referenced (RSE)</td><td> 
</td><td>NOT RECOMMENDED
 

Ground-loop losses, V_g, are added to measured signal.</td></tr>
<tr><td>Single-Ended — Nonreferenced (NRSE)</td><td> 

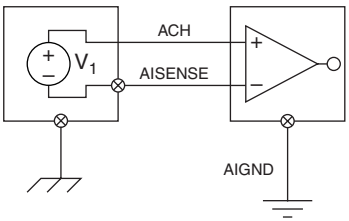
See text for information on bias resistors.</td><td> 
</td></tr>
</table>

Figure 4-3. Summary of Analog Input Connections

Differential Connection Considerations (DIFF Input Configuration)

A differential connection is one in which the AI signal has its own reference signal or signal return path. These connections are available when the selected channel is configured in DIFF mode. In DIFF mode, the AI channels are paired, with ACH<*i*> as the signal input and ACH<*i*+8> as the signal reference. For example, ACH0 is paired with ACH8, ACH1 is paired with ACH9, and so on. The input signal connects to the positive input of the PGIA, and its reference signal, or return, connects to the negative input of the PGIA.

When you configure a channel for differential input, each signal uses two multiplexer inputs—one for the signal and one for the channel reference signal. Therefore, with a differential configuration for every channel, up to eight AI channels are available.

You should use differential input connections for channels that meet any of the following conditions:

- The input signal is low level (less than 1 V).
- The leads connecting the signal to the DAQCard-6062E are greater than 3 m (10 ft).
- The input signal requires a separate ground-reference point or return signal.
- The signal leads travel through noisy environments.

Differential signal connections reduce picked-up noise and increase common-mode noise rejection. Differential signal connections also allow input signals to float within the common-mode limits of the PGIA.

Differential Connections for Ground-Referenced Signal Sources

Figure 4-4 shows how to connect a ground-referenced signal source to a channel on a DAQCard-6062E configured in DIFF mode.

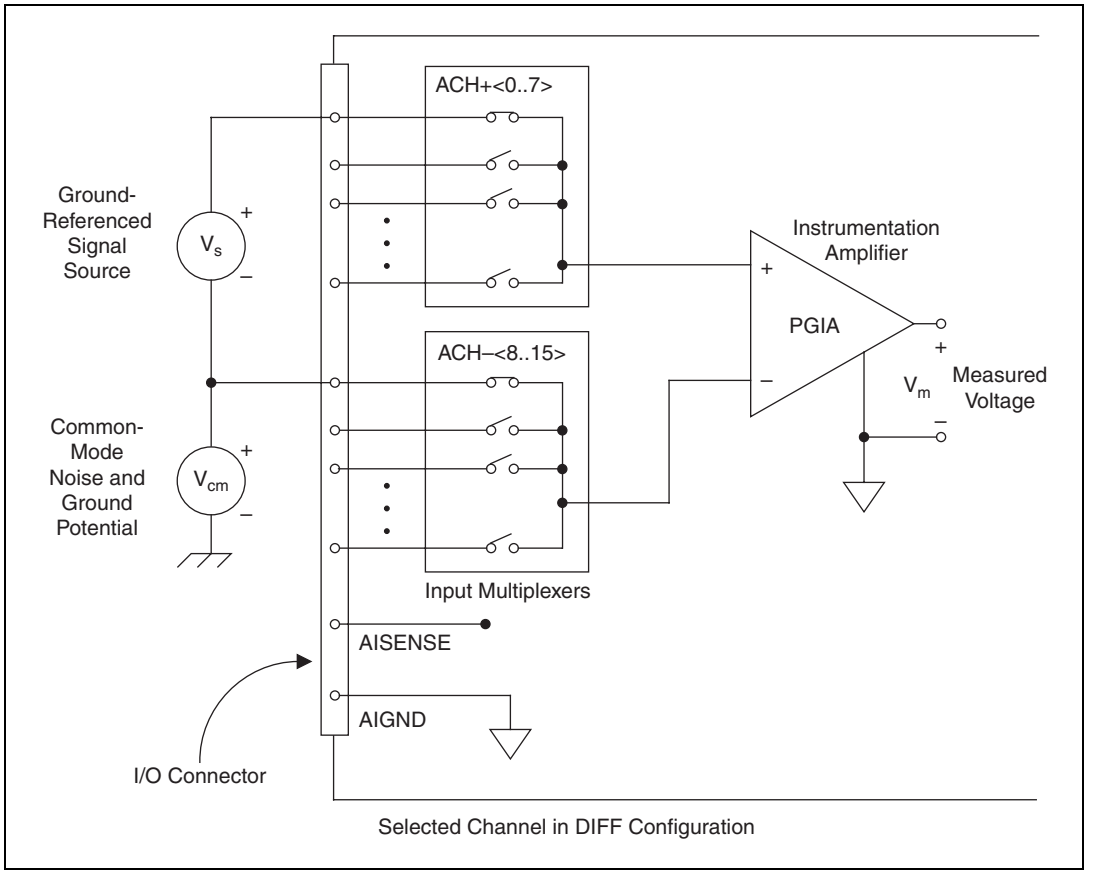


Figure 4-4. Differential Input Connections for Ground-Referenced Signals

With this type of connection, the PGIA rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the DAQCard-6062E ground, shown as V_{cm} in Figure 4-4.

Differential Connections for Nonreferenced or Floating Signal Sources

Figure 4-5 shows how to connect a floating signal source to a channel on a DAQCard-6062E configured in DIFF mode.

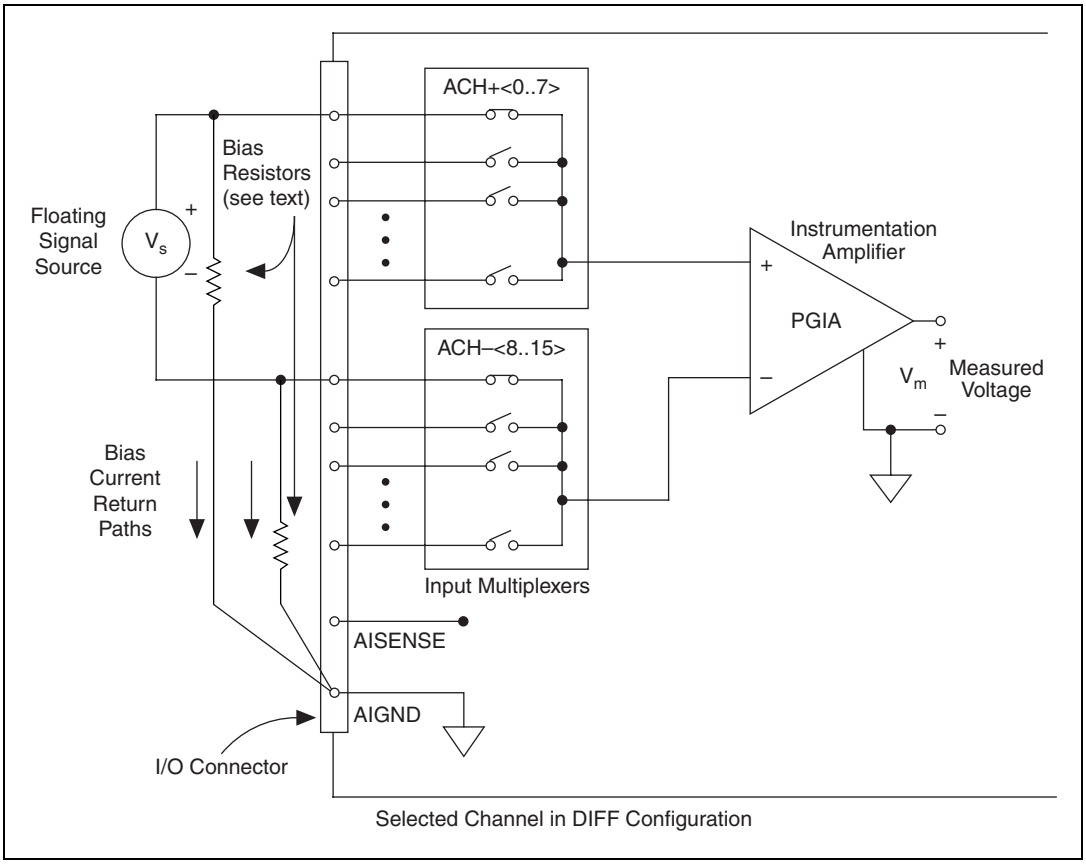


Figure 4-5. Differential Input Connections for Nonreferenced Signals

Figure 4-5 shows two bias resistors connected in parallel with the signal leads of a floating signal source. If you do not use the resistors and the source is truly floating, the source is unlikely to remain within the common-mode signal range of the PGIA, and the PGIA saturates, causing erroneous readings. You must reference the source to AIGND. The easiest way is to connect the positive side of the signal to the positive input of the

PGIA and connect the negative side of the signal to AIGND as well as to the negative input of the PGIA, without any resistors. This connection works well for DC-coupled sources with low source impedance (less than 100 Ω).

However, for larger source impedances, this connection leaves the differential signal path significantly off balance. Noise that couples electrostatically onto the positive line does not couple onto the negative line because it is connected to ground. Therefore, this noise appears as a differential-mode signal instead of a common-mode signal, and the PGIA does not reject it. In this case, instead of directly connecting the negative line to AIGND, connect it to AIGND through a resistor that is about 100 times the equivalent source impedance. The resistor puts the signal path nearly in balance, so that about the same amount of noise couples onto both connections, yielding better rejection of electrostatically coupled noise. Also, this configuration does not load down the source (other than the very high-input impedance of the PGIA).

You can fully balance the signal path by connecting another resistor of the same value between the positive input and AIGND, as shown in Figure 4-5. This fully balanced configuration offers slightly better noise rejection but has the disadvantage of loading the source down with the series combination (sum) of the two resistors. If, for example, the source impedance is 2 kΩ and each of the two resistors is 100 kΩ, the resistors load down the source with 200 kΩ and produce a –1% gain error.

Both inputs of the PGIA require a DC path to ground in order for the PGIA to work. If the source is AC coupled (capacitively coupled), the PGIA needs a resistor between the positive input and AIGND. If the source has low impedance, choose a resistor that is large enough not to significantly load the source but small enough not to produce significant input offset voltage as a result of input bias current (typically 100 kΩ to 1 MΩ). In this case, you can connect the negative input directly to AIGND. If the source has high output impedance, balance the signal path as previously described using the same value resistor on both the positive and negative inputs; be aware that there is some gain error from loading down the source.

Single-Ended Connection Considerations

In a single-ended connection, the AI signal is referenced to a ground that can be shared with other input signals. The input signal connects to the positive input of the PGIA, and the ground connects to the negative input of the PGIA.

When every channel is configured for single-ended input, up to 16 AI channels on the NI 6052E are available. Use single-ended input connections for any input signal that meets the following conditions:

- The input signal is high level (greater than 1 V).
- The leads connecting the signal to the device are less than 3 m (10 ft).
- The input signal can share a common reference point with other signals.

DIFF input connections are recommended for greater signal integrity for input signals that do not meet the preceding conditions.

Using application software, you can configure the NI 6052E channels for RSE or NRSE mode. RSE mode is used for floating signal sources. In this case, the NI 6052E provides the reference ground point for the external signal. NRSE mode is used for ground-referenced signal sources. In this case, the external signal supplies its own reference ground point, and the device should not supply one.

In single-ended configurations, more electrostatic and magnetic noise couples into the signal connections than in the DIFF configuration. The coupling is a result of signal path differences. Magnetic coupling is proportional to the area between the two signal conductors. Electrical coupling is a function of how much the electric field differs between the two signal conductors.

Single-Ended Connections for Floating Signal Sources (RSE Configuration)

Figure 4-6 shows how to connect a floating signal source to a channel on a DAQCard-6062E configured for RSE mode.

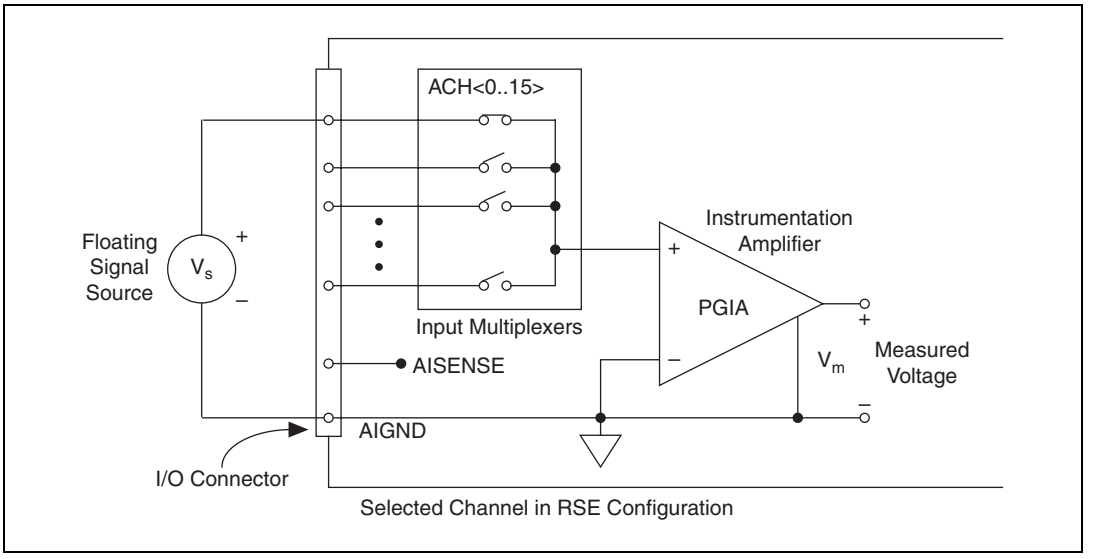


Figure 4-6. Single-Ended Input Connections for Nonreferenced or Floating Signals

Single-Ended Connections for Grounded Signal Sources (NRSE Configuration)

To measure a grounded signal source with a single-ended configuration, you must configure the DAQCard-6062E for the NRSE mode. The signal then connects to the positive input of the DAQCard PGIA, and the signal local ground reference connects to the negative input of the PGIA. The ground point of the signal should, therefore, connect to the AISENSE pin. Any potential difference between the DAQCard-6062E ground and the signal ground appears as a common-mode signal at both the positive and negative inputs of the PGIA, and the amplifier rejects this difference. If the input circuitry of a DAQCard-6062E were referenced to ground, in this situation as in the RSE input configuration, this difference in ground potentials appears as an error in the measured voltage.

Figure 4-7 shows how to connect a grounded signal source to a channel on a DAQCard-6062E configured for NRSE mode.

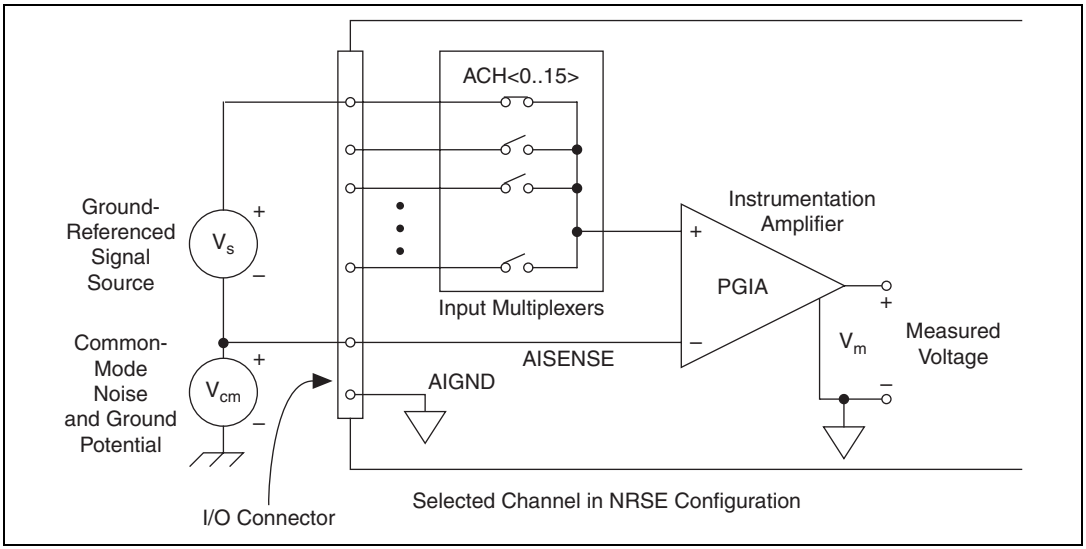


Figure 4-7. Single-Ended Input Connections for Ground-Referenced Signals

Common-Mode Signal Rejection Considerations

Figures 4-4 and 4-7 show connections for signal sources that are already referenced to some ground point with respect to the DAQCard-6062E. In these cases, the PGIA can reject any voltage caused by ground potential differences between the signal source and the DAQCard-6062E.
In addition, with differential input connections, the PGIA can reject common-mode noise pickup in the leads connecting the signal sources to the DAQCard-6062E. The PGIA can reject common-mode signals as long as V_{in}+ and V_{in}– are both within ±11 V of AIGND.

Analog Output Signal Connections

The AO signals are DAC0OUT, DAC1OUT, EXTREF, and AOGND.

- DAC0OUT is the voltage output signal for AO channel 0.
- DAC1OUT is the voltage output signal for AO channel 1.

EXTREF is the external reference input for both AO channels. You must individually configure each AO channel for external reference selection in order for the signal applied at the external reference input to be used by that

channel. If you do not specify an external reference, the channel uses the internal reference. AO configuration options are explained in the *Analog Input* section of Chapter 3, *Hardware Overview*. The following ranges and ratings apply to the EXTREF input:

- Usable input voltage range: ±11 V peak with respect to AOGND
- Absolute maximum ratings: ±15 V peak with respect to AOGND

AOGND is the ground reference signal for both AO channels and the external reference signal.

Figure 4-8 shows how to make AO connections and the external reference input connection to the DAQCard-6062E.

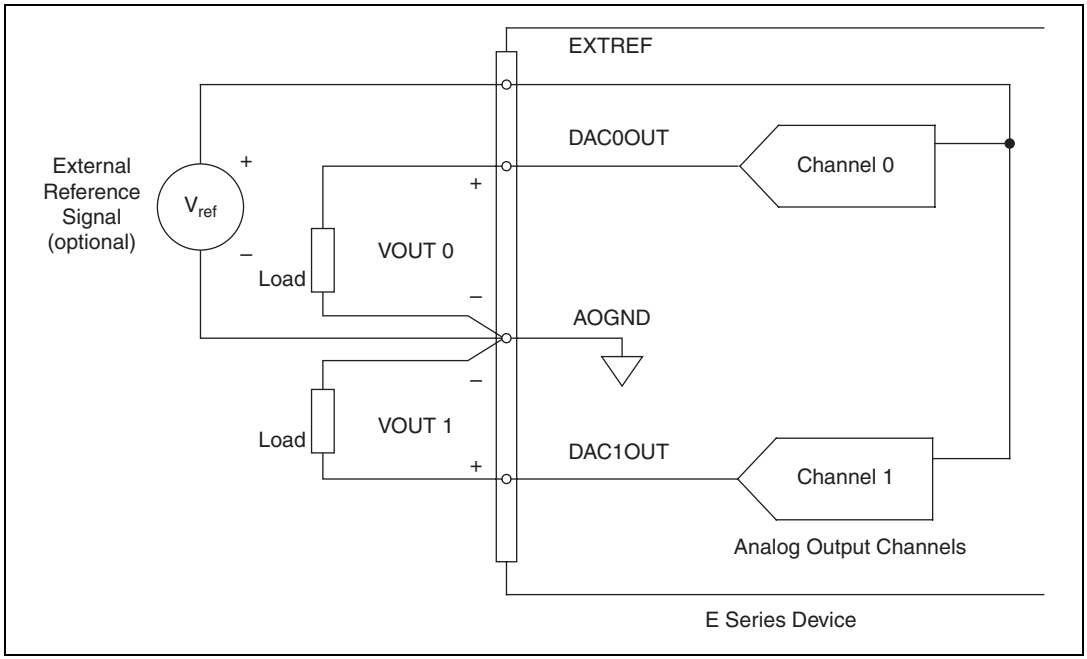


Figure 4-8. Analog Output Connections

The external reference signal can be either a DC signal or an AC signal. The device multiplies this reference signal by the DAC code (divided by the full-scale DAC code) to generate the output voltage.

Connecting Digital I/O Signals

The DIO signals are DIO<0..7> and DGND. The DIO<0..7> signals make up the DIO port, and DGND is the ground reference signal for this port. You can individually program all lines as inputs or outputs.

Caution Exceeding the maximum input voltage ratings, which are listed in Table 4-3, can damage the DAQCard-6062E and the computer. NI is *not* liable for any damage resulting from such signal connections.

Figure 4-9 shows signal connections for three typical DIO applications.

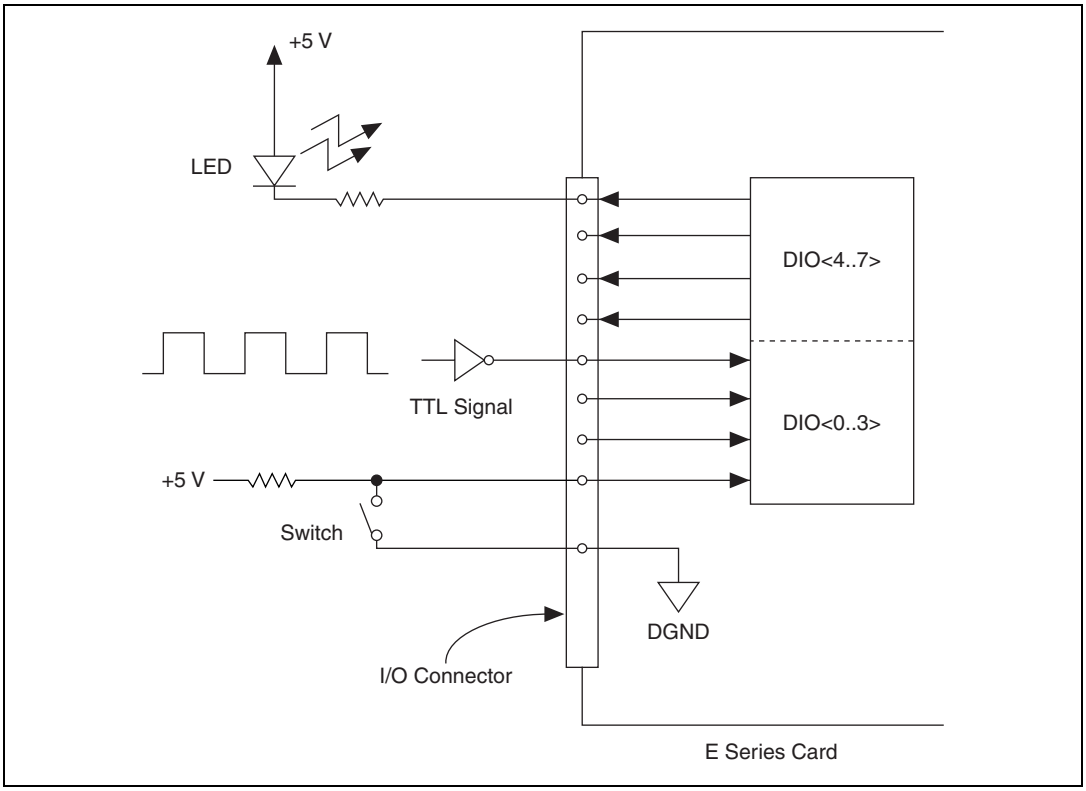


Figure 4-9. Digital I/O Connections

Figure 4-9 shows DIO<0..3> configured for digital input, and DIO<4..7> configured for digital output. Digital input applications include receiving TTL signals and sensing external device states, such as the state of the

switch shown in the figure. Digital output applications include sending TTL signals and driving external devices, such as the LED shown in the figure.

Power Connections

Two pins on the I/O connector supply +5 V from the computer power supply through a self-resetting fuse. The fuse resets automatically within a few seconds after the overcurrent condition is removed. These pins are referenced to DGND, and you can use them to power external digital circuitry.

Refer to the power requirement of the I/O connection supply in Appendix A, *Specifications*, for more information on powering the device.

Caution Do *not*, under any circumstances, connect these +5 V power pins directly to analog or digital ground or to any other voltage source on the DAQCard-6062E or any other device. Doing so can damage the DAQCard-6062E and the computer. NI is *not* liable for damage resulting from such a connection.

Connecting Timing Signals

Caution Exceeding the maximum input voltage ratings, which are listed in Table 4-3, can damage the DAQCard-6062E and the computer. NI is *not* liable for any damage resulting from such signal connections.

All external control of the DAQCard-6062E timing is routed through the 10 PFIs, labeled PFI0 through PFI9. These signals are explained in detail in the *Programmable Function Input Connections* section. These PFIs are bidirectional; as outputs they are not programmable and reflect the state of many DAQ, waveform generation, and general-purpose timing signals. There are five other dedicated outputs for the remainder of the timing signals. As inputs, the PFIs are programmable and can control any DAQ, waveform generation, and general-purpose timing signals.

The *Data Acquisition Timing Connections* section explains the DAQ signals. The *Waveform Generation Timing Connections* section explains waveform generation signals. The *General-Purpose Timing Signal Connections* section explains the general-purpose timing signals.

All digital timing connections are referenced to DGND. This reference is demonstrated in Figure 4-10, which shows how to connect an external TRIG1 source and an external CONVERT* source to two of the DAQCard-6062E PFI pins.

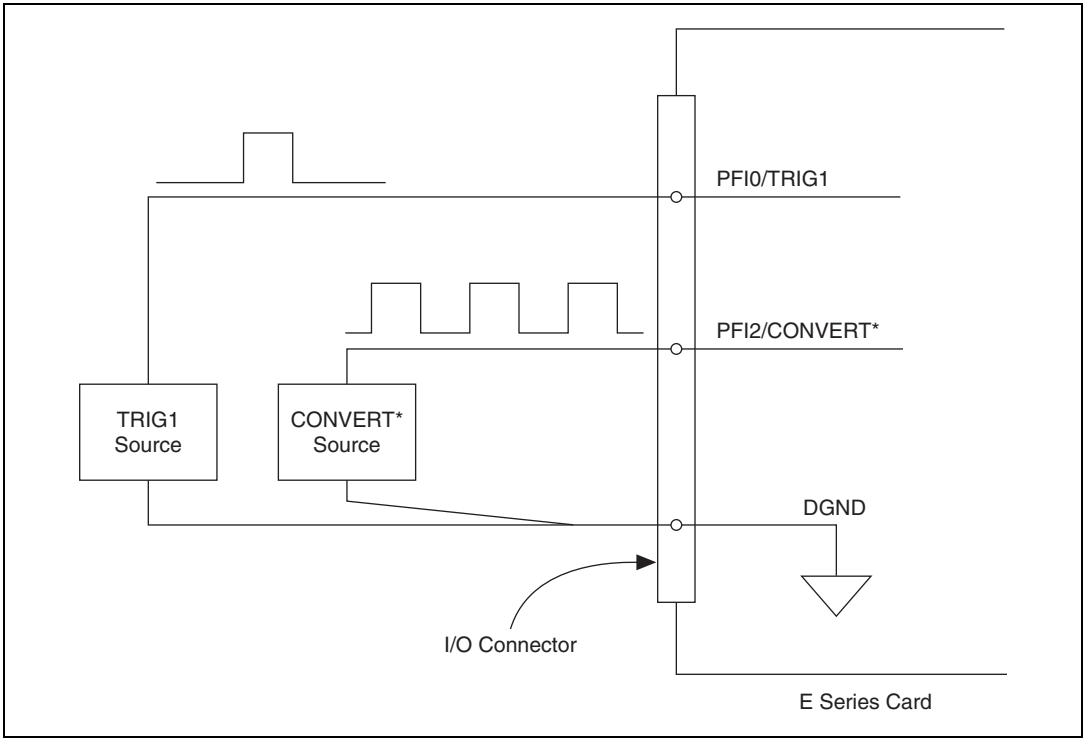


Figure 4-10. Timing I/O Connections

Programmable Function Input Connections

You can externally control 13 internal timing signals from the PFI pins. The source for each of these signals is software selectable from any PFI when you want external control. This flexible routing scheme reduces the need to change the physical wiring to the DAQCard-6062E I/O connector for different applications requiring alternative wiring.

You can individually enable each PFI pin to output a specific internal timing signal. For example, if you need the CONVERT* signal as an output on the I/O connector, software can turn on the output driver for the PFI2/CONVERT* pin. Be careful not to drive a PFI signal externally when it is configured as an output.

As an input, each PFI can be individually configured for edge or level detection and for polarity selection. You can use the polarity selection for any of the timing signals, but the edge or level detection depends upon the particular timing signal being controlled. The detection requirements for each timing signal are listed within the section that discusses that individual signal.

In edge-detection mode, the minimum pulse width required is 10 ns. This requirement applies for both rising-edge and falling-edge polarity settings. Edge-detection mode does not have a maximum pulse-width requirement.

In level-detection mode, no minimum or maximum pulse-width requirements are imposed by the PFIs themselves, but limits may be imposed by the particular timing signal being controlled. These requirements are listed later in this chapter.

Data Acquisition Timing Connections

The data acquisition timing signals are TRIG1, TRIG2, STARTSCAN, CONVERT*, AIGATE, SISOURCE, SCANCLK, and EXTSTROBE*.

Posttriggered data acquisition allows you to view only data that is acquired after a trigger event is received. A typical posttriggered DAQ sequence is shown in Figure 4-11.

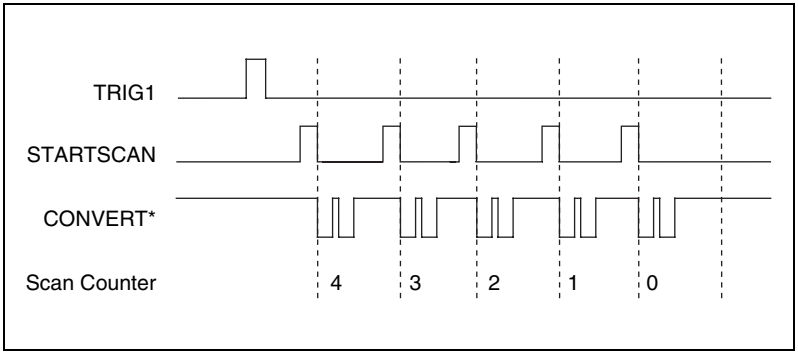


Figure 4-11. Typical Posttriggered Acquisition

Pretriggered data acquisition allows you to view data that is acquired before the trigger of interest in addition to data acquired after the trigger. Figure 4-12 shows a typical pretriggered DAQ sequence.

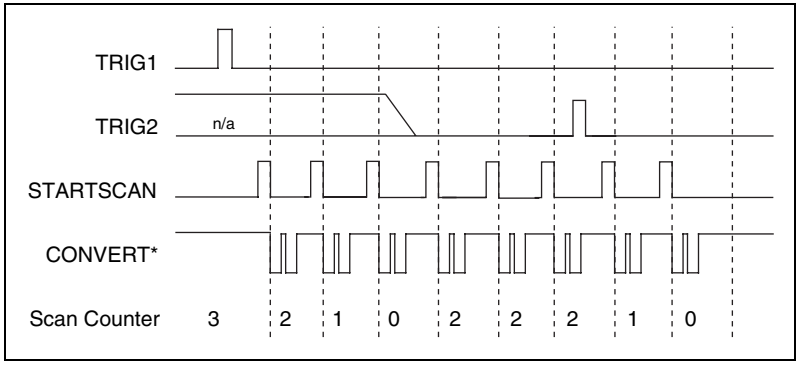


Figure 4-12. Typical Pretriggered Acquisition

The description for each signal shown in these figures is included in this chapter.

TRIG1 Signal

Any PFI pin can externally input the TRIG1 signal, which is available as an output on the PFI0/TRIG1 pin.

Refer to Figures 4-11 and 4-12 for the relationship of TRIG1 to the DAQ sequence.

As an input, TRIG1 is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG1 and configure the polarity selection for either rising or falling edge. The selected edge of TRIG1 starts the DAQ sequence for both posttriggered and pretriggered acquisitions. The DAQCard-6062E supports analog triggering on the PFI0/TRIG1 pin. Refer to Chapter 3, *Hardware Overview*, for more information on analog triggering.

As an output, TRIG1 reflects the action that initiates a DAQ sequence, even if another PFI externally triggers the acquisition. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures 4-13 and 4-14 show the timing requirements for TRIG1.

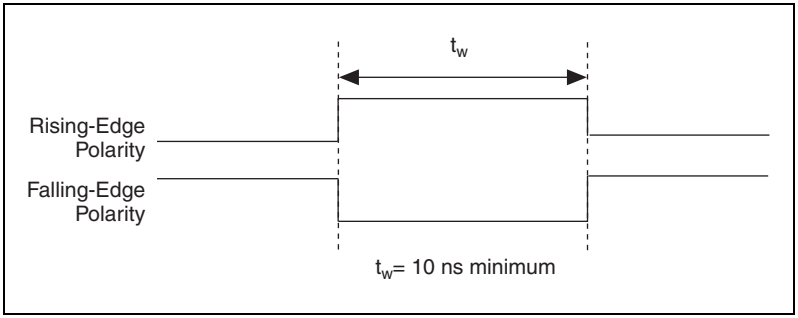


Figure 4-13. TRIG1 Input Signal Timing

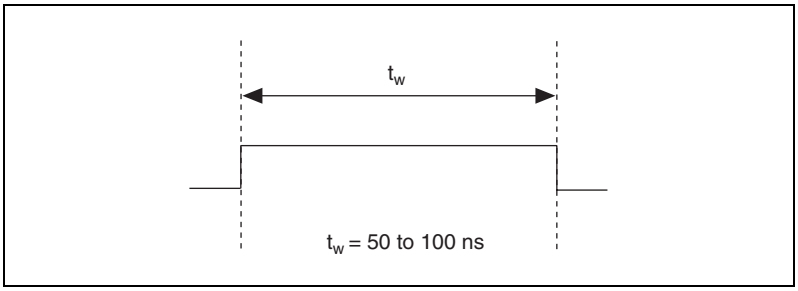


Figure 4-14. TRIG1 Output Signal Timing

The DAQCard-6062E also uses TRIG1 to initiate pretriggered DAQ operations. In most pretriggered applications, TRIG1 is generated by a software trigger. Refer to the TRIG2 signal description for a complete description of the use of TRIG1 and TRIG2 in a pretriggered DAQ operation.

TRIG2 Signal

Any PFI pin can externally input the TRIG2 signal, which is available as an output on the PFI1/TRIG2 pin.

Refer to Figure 4-12 for the relationship of TRIG2 to the DAQ sequence.

As an input, TRIG2 is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG2 and configure the polarity selection for either rising or falling edge. The selected edge of TRIG2 initiates the posttriggered phase of a pretriggered DAQ sequence. In pretriggered mode, the TRIG1 signal initiates the acquisition. The scan counter (SC) indicates the minimum number of scans before TRIG2 is

recognized. After the SC decrements to zero, it is loaded with the number of posttrigger scans to acquire while the acquisition continues. The DAQCard-6062E ignores TRIG2 if it is asserted prior to the SC decrementing to zero. After the selected edge of TRIG2 is received, the DAQCard-6062E acquires a fixed number of scans and the acquisition stops. This mode acquires data both before and after receiving TRIG2.

As an output, TRIG2 reflects the posttrigger in a pretriggered DAQ sequence, even if another PFI externally triggers the acquisition. TRIG2 is not used in posttriggered acquisitions. The output is an active high pulse with a pulse width of 50 to 100 ns. This signal is set to high-impedance at startup.

Figures 4-15 and 4-16 show the input and output timing requirements for TRIG2.

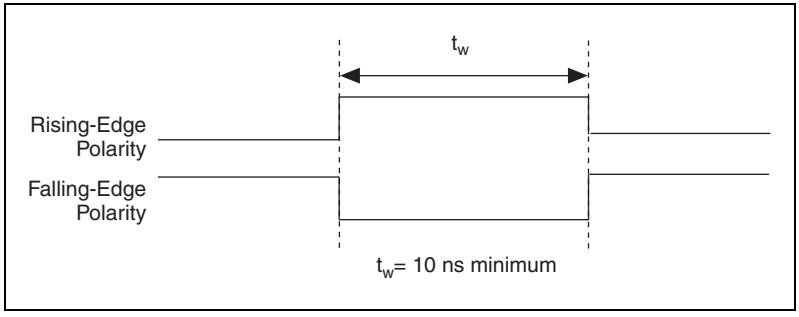


Figure 4-15. TRIG2 Input Signal Timing

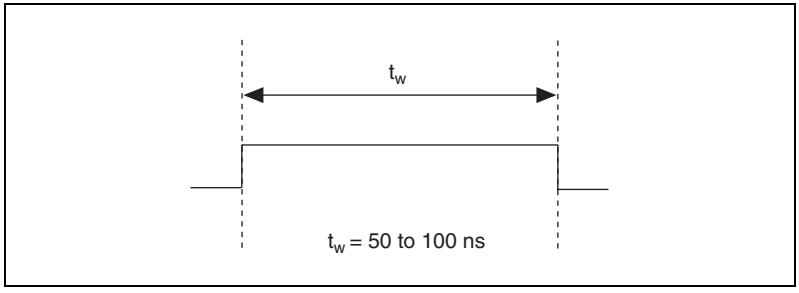


Figure 4-16. TRIG2 Output Signal Timing

STARTSCAN Signal

Any PFI pin can externally input the STARTSCAN signal, which is available as an output on the PFI7/STARTSCAN pin.

Refer to Figures 4-11 and 4-12 for the relationship of STARTSCAN to the DAQ sequence.

As an input, STARTSCAN is configured in the edge-detection mode. You can select any PFI pin as the source for STARTSCAN and configure the polarity selection for either rising or falling edge. The selected edge of the STARTSCAN signal initiates a scan. The sample interval (SI2) counter is started if you select internally triggered CONVERT*.

As an output, STARTSCAN reflects the actual start pulse that initiates a scan, even if another PFI externally triggers the starts. You have two output options. The first option is an active high pulse with a pulse width of 50 to 100 ns, which indicates the start of the scan. The second option is an active high pulse that terminates at the start of the last conversion in the scan, which indicates a scan in progress. STARTSCAN is deasserted, t_{off} after the last conversion in the scan is initiated. This output is set to high-impedance at startup.

Figures 4-17 and 4-18 show the timing requirements for STARTSCAN.

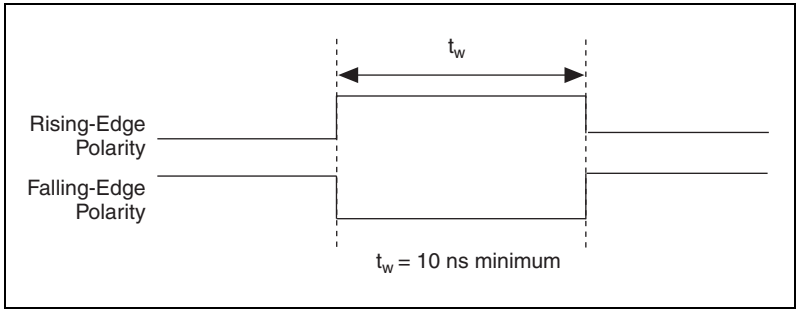


Figure 4-17. STARTSCAN Input Signal Timing

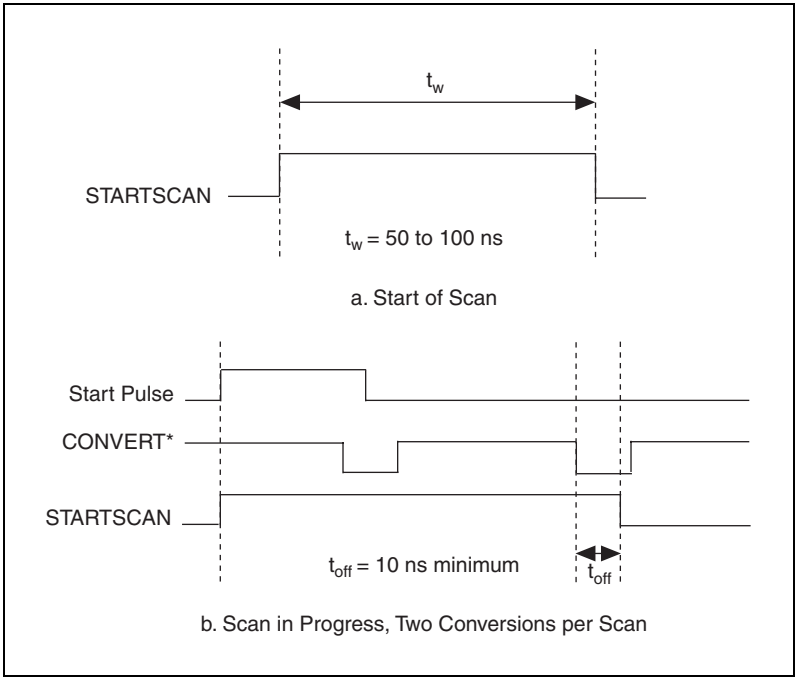


Figure 4-18. STARTSCAN Output Signal Timing

The CONVERT* pulses are masked off until the DAQCard-6062E generates the STARTSCAN signal. If you are using internally generated conversions, the first CONVERT* will appear when the onboard SI2 counter reaches zero. If you select an external CONVERT*, the first external pulse after STARTSCAN generates a conversion. STARTSCAN pulses should be separated by at least one scan period.

A counter on the DAQCard-6062E internally generates the STARTSCAN signal unless you select some external source. This counter is started by the TRIG1 signal and is stopped either by software or by the sample counter.

Scans generated by either an internal or external STARTSCAN signal are inhibited unless they occur within a DAQ sequence. Scans occurring within a DAQ sequence may be gated by either the hardware signal AIGATE or the software command register gate.

CONVERT* Signal

Any PFI pin can externally input the CONVERT* signal, which is available as an output on the PFI2/CONVERT* pin.

Refer to Figures 4-11 and 4-12 for the relationship of CONVERT* to the DAQ sequence.

As an input, CONVERT* is configured in the edge-detection mode. You can select any PFI pin as the source for CONVERT* and configure the polarity selection for either rising or falling edge. The selected edge of CONVERT* initiates an A/D conversion.

As an output, CONVERT* reflects the actual convert pulse that connects to the ADC, even if the conversions are externally generated by another PFI. The output is an active low pulse with a pulse width of 50 to 100 ns. This signal is set to high-impedance at startup.

Figures 4-19 and 4-20 show the timing requirements for CONVERT*.

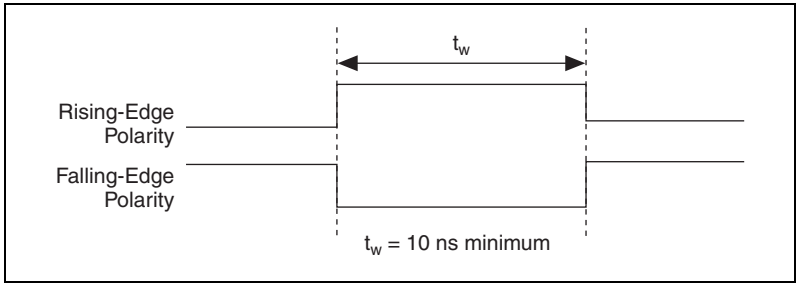


Figure 4-19. CONVERT* Input Signal Timing

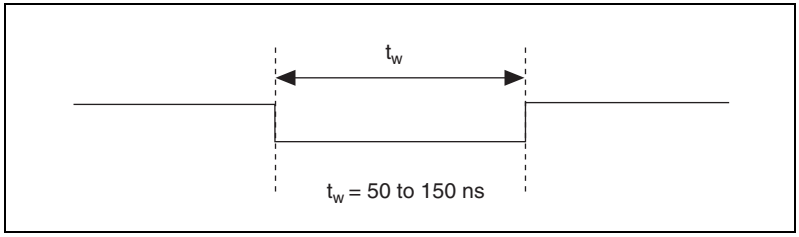


Figure 4-20. CONVERT* Output Signal Timing

The ADC switches to hold mode within 60 ns of the selected edge. This hold-mode delay time is a function of temperature and does not vary from one conversion to the next. Separate the CONVERT* pulses by at least one conversion period.

The SI2 counter on the DAQCard-6062E normally generates CONVERT* unless you select some external source. The counter is started by the STARTSCAN signal and continues to count down and reload itself until the scan is finished. It then reloads itself in readiness for the next STARTSCAN pulse.

A/D conversions generated by either an internal or external CONVERT* signal are inhibited unless they occur within a DAQ sequence. Scans occurring within a DAQ sequence may be gated by either the hardware signal AIGATE or the software command register gate.

AIGATE Signal

Any PFI pin can externally input the AIGATE signal, which is not available as an output on the I/O connector. The AIGATE signal can mask off scans in a DAQ sequence. You can configure the PFI pin you select as the source for the AIGATE signal in level-detection mode. In the level-detection mode if AIGATE is active, the STARTSCAN signal is masked off, and no scans can occur. You can configure the polarity selection for the PFI pin for either active high or active low.

The AIGATE signal can neither stop a scan in progress nor continue a previously gated-off scan; in other words, once a scan has started, AIGATE does not gate-off conversions until the beginning of the next scan and, conversely, if conversions are gated off, AIGATE does not gate them back on until the beginning of the next scan.

SISOURCE Signal

Any PFI pin can externally input the SISOURCE signal, which is not available as an output on the I/O connector. The onboard scan interval (SI) counter uses the SISOURCE signal as a clock to time the generation of the STARTSCAN signal. You must configure the PFI pin you select as the source for SISOURCE in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase generates SISOURCE unless you select some external source. Figure 4-21 shows the timing requirements for SISOURCE.

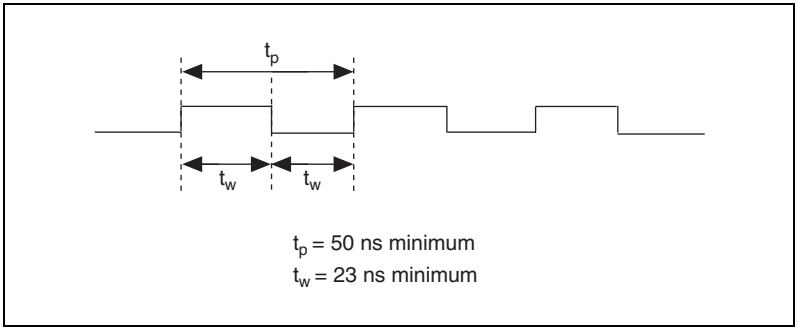


Figure 4-21. SISOURCE Signal Timing

SCANCLK Signal

SCANCLK is an output-only signal that generates a pulse with the leading edge occurring approximately 50 to 100 ns after an A/D conversion begins. The polarity of this output is software selectable but is typically configured so that a low-to-high leading edge can clock external AI multiplexers indicating when the input signal has been sampled and can be removed. This signal has a 400 to 500 ns pulse width and is software enabled.

Note When using NI-DAQ, SCANCLK polarity is low-to-high, and you cannot change it programmatically.

Figure 4-22 shows the timing for SCANCLK.

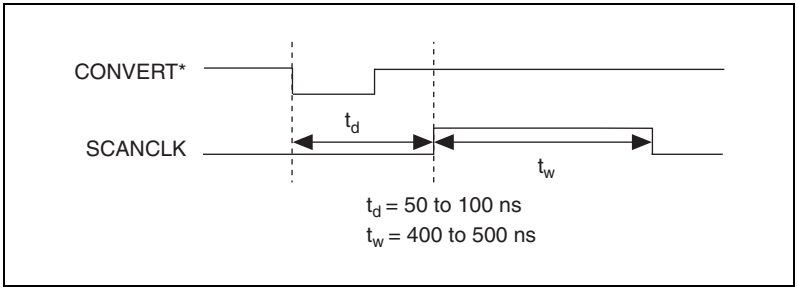


Figure 4-22. SCANCLK Signal Timing

EXTSTROBE* Signal

EXTSTROBE* is an output-only signal that generates either a single pulse or a sequence of eight pulses in the hardware-strobe mode. An external device can use this signal to latch signals or to trigger events. In the single-pulse mode, software controls the level of the EXTSTROBE* signal. Both 10 µs and 1.2 µs clocks are available for generating a sequence of eight pulses in the hardware-strobe mode.

Note You cannot control EXTROBE* using NI-DAQ.

Figure 4-23 shows the timing for the hardware-strobe mode EXTSTROBE* signal.

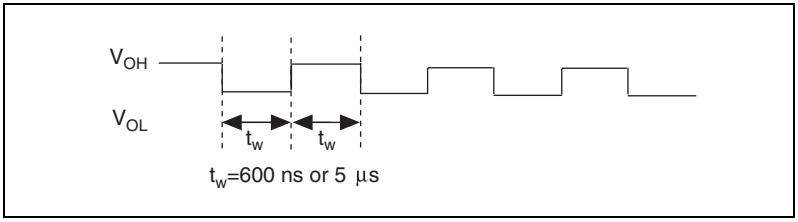


Figure 4-23. EXTSTROBE* Signal Timing

Waveform Generation Timing Connections

The analog group defined for the DAQCard-6062E is controlled by WFTRIG, UPDATE*, and UISOURCE.

WFTRIG Signal

Any PFI pin can externally input the WFTRIG signal, which is available as an output on the PFI6/WFTRIG pin.

As an input, WFTRIG is configured in the edge-detection mode. You can select any PFI pin as the source for WFTRIG and configure the polarity selection for either rising or falling edge. The selected edge of WFTRIG starts the waveform generation for the DACs. The update interval (UI) counter is started if you select internally generated UPDATE*.

As an output, WFTRIG reflects the trigger that initiates waveform generation, even if another PFI externally triggers the waveform generation. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures 4-24 and 4-25 show the input and output timing requirements for the WFTRIG signal.

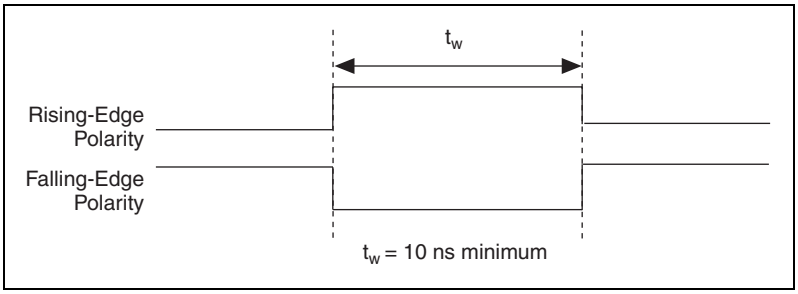


Figure 4-24. WFTRIG Input Signal Timing

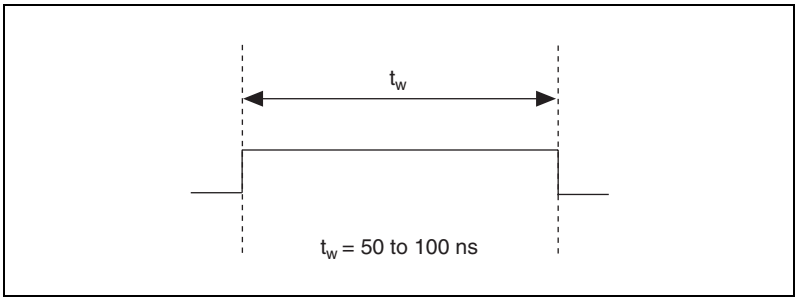


Figure 4-25. WFTRIG Output Signal Timing

UPDATE* Signal

Any PFI pin can externally input the UPDATE* signal, which is available as an output on the PFI5/UPDATE* pin.

As an input, UPDATE* is configured in the edge-detection mode. You can select any PFI pin as the source for UPDATE* and configure the polarity selection for either rising or falling edge. The selected edge of UPDATE* updates the outputs of the DACs. In order to use UPDATE*, you must set the DACs to posted-update mode.

As an output, UPDATE* reflects the actual update pulse that is connected to the DACs, even if another PFI externally generates the updates. The output is an active low pulse with a pulse width of 300 to 350 ns. This output is set to high-impedance at startup.

Figures 4-26 and 4-27 show the input and output timing requirements for the UPDATE* signal.

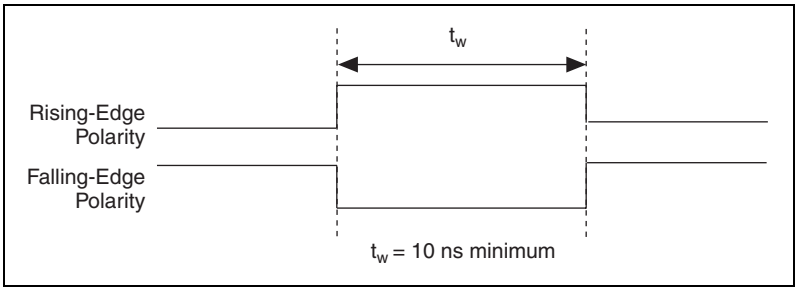


Figure 4-26. UPDATE* Input Signal Timing

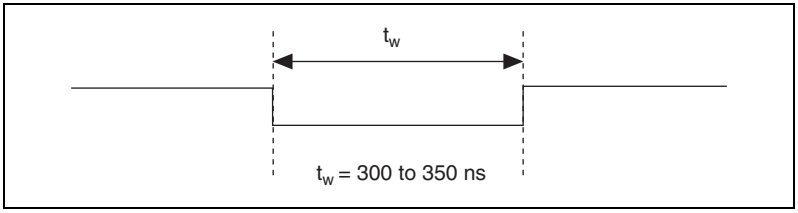


Figure 4-27. UPDATE* Output Signal Timing

The DACs are updated within 1.3 µs of the leading edge. Separate the UPDATE* pulses with enough time that new data can be written to the DAC latches.

The UI counter normally generates the UPDATE* signal unless you select some external source. The UI counter is started by the WFTRIG signal and can be stopped by software or the internal buffer counter (BC).

D/A conversions generated by either an internal or external UPDATE* signal do not occur when gated by the software command register gate.

UISOURCE Signal

Any PFI pin can externally input the UISOURCE signal, which is not available as an output on the I/O connector. The UI counter uses the UISOURCE signal as a clock to time the generation of UPDATE*. You must configure the PFI pin you select as the source for the UISOURCE signal in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low. Figure 4-28 shows the timing requirements for UISOURCE.

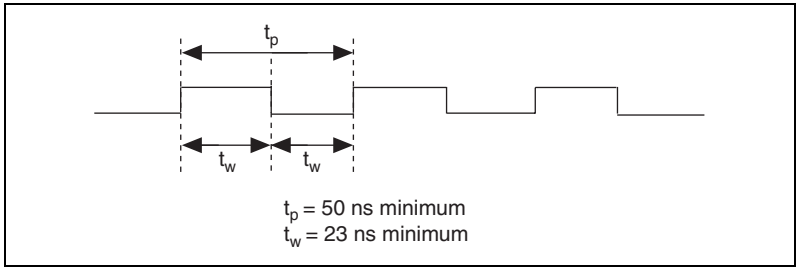


Figure 4-28. UISOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase normally generates UISOURCE unless you select some external source.

General-Purpose Timing Signal Connections

The general-purpose timing signals are GPCTR0_SOURCE, GPCTR0_GATE, GPCTR0_OUT, GPCTR0_UP_DOWN, GPCTR1_SOURCE, GPCTR1_GATE, GPCTR1_OUT, GPCTR1_UP_DOWN, and FREQ_OUT.

GPCTR0_SOURCE Signal

Any PFI pin can externally input the GPCTR0_SOURCE signal, which is available as an output on the PFI8/GPCTR0_SOURCE pin.

As an input, GPCTR0_SOURCE is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, GPCTR0_SOURCE reflects the actual clock connected to general-purpose counter 0, even if another PFI externally inputs the source clock. This signal is set to high-impedance at startup.

Figure 4-29 shows the timing requirements for GPCTR0_SOURCE.

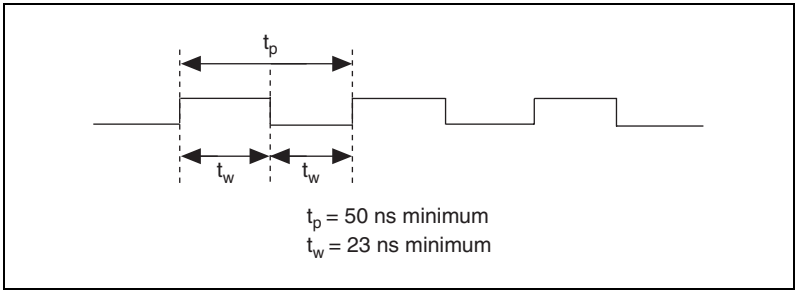


Figure 4-29. GPCTR0_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates GPCTR0_SOURCE unless you select some external source.

GPCTR0_GATE Signal

Any PFI pin can externally input the GPCTR0_GATE signal, which is available as an output on the PFI9/GPCTR0_GATE pin.

As an input, GPCTR0_GATE is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of applications to perform actions such as starting and stopping the counter, generating interrupts, and saving the counter contents.

As an output, GPCTR0_GATE reflects the actual gate signal connected to general-purpose counter 0, even if another PFI externally generates the gate. This signal is set to high-impedance at startup.

Figure 4-30 shows the timing requirements for GPCTR0_GATE.

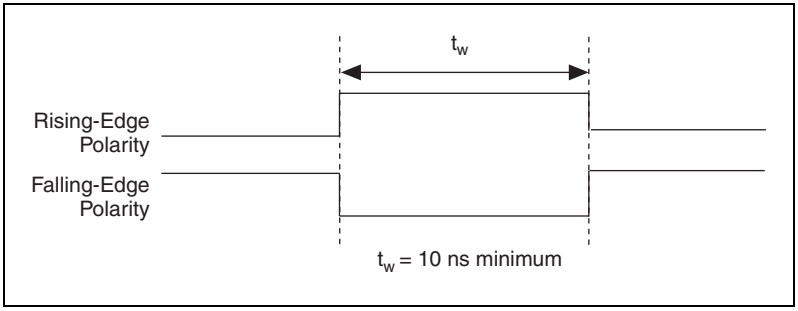


Figure 4-30. GPCTR0_GATE Signal Timing in Edge-Detection Mode

GPCTR0_OUT Signal

This signal is available only as an output on the GPCTR0_OUT pin. The GPCTR0_OUT signal reflects the terminal count (TC) of general-purpose counter 0. You have two software-selectable output options: pulse on TC and toggle output polarity on TC. The output polarity is software selectable for both options. This signal is set to high-impedance at startup.
Figure 4-31 shows the timing of GPCTR0_OUT.

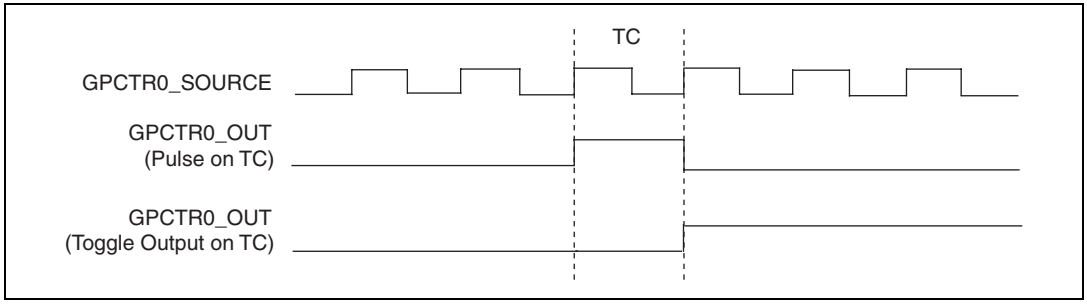


Figure 4-31. GPCTR0_OUT Signal Timing

GPCTR0_UP_DOWN Signal

This signal can be externally input on the DIO6 pin and is not available as an output on the I/O connector. The general-purpose counter 0 counts down when this pin is at a logic low and count up when it is at a logic high. You can disable this input so that software can control the up/down functionality and leave the DIO6 pin free for general use.

GPCTR1_SOURCE Signal

Any PFI pin can externally input the GPCTR1_SOURCE signal, which is available as an output on the PFI3/GPCTR1_SOURCE pin.

As an input, GPCTR1_SOURCE is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR1_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, GPCTR1_SOURCE monitors the actual clock connected to general-purpose counter 1, even if another PFI externally generates the source clock. This signal is set to high-impedance at startup.

Figure 4-32 shows the timing requirements for GPCTR1_SOURCE.

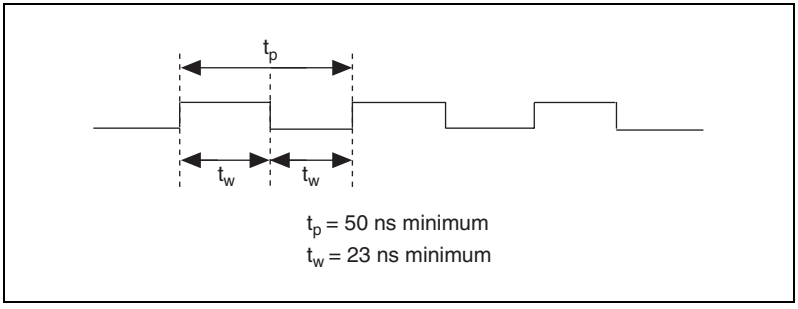


Figure 4-32. GPCTR1_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates GPCTR1_SOURCE unless you select some external source.

GPCTR1_GATE Signal

Any PFI pin can externally input the GPCTR1_GATE signal, which is available as an output on the PFI4/GPCTR1_GATE pin.

As an input, the GPCTR1_GATE signal is configured in edge-detection mode. You can select any PFI pin as the source for GPCTR1_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform actions such as starting and stopping the counter, generating interrupts, and saving the counter contents.

As an output, GPCTR1_GATE monitors the actual gate signal connected to general-purpose counter 1, even if another PFI externally generates the gate. This signal is set to high-impedance at startup.

Figure 4-33 shows the timing requirements for GPCTR1_GATE.

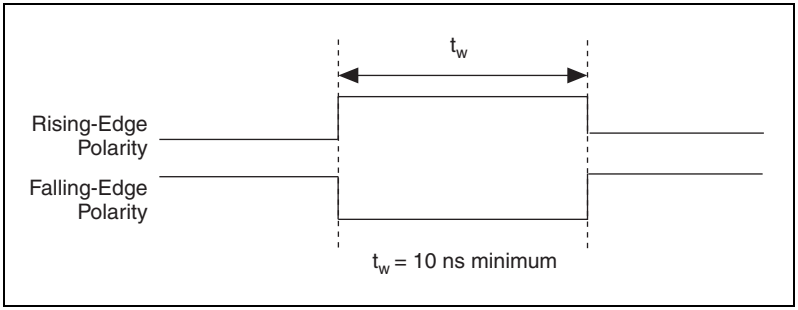


Figure 4-33. GPCTR1_GATE Signal Timing in Edge-Detection Mode

GPCTR1_OUT Signal

This signal is available only as an output on the GPCTR1_OUT pin. The GPCTR1_OUT signal monitors the TC device general-purpose counter 1. You have two software-selectable output options: pulse on TC and toggle output polarity on TC. The output polarity is software-selectable for both options. This signal is set to high-impedance at startup. Figure 4-34 shows the timing requirements for GPCTR1_OUT.

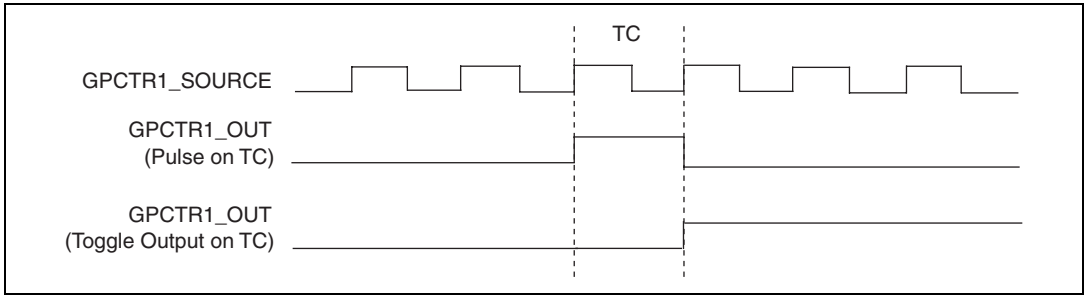


Figure 4-34. GPCTR1_OUT Signal Timing

GPCTR1_UP_DOWN Signal

This signal can be externally input on the DIO7 pin and is not available as an output on the I/O connector. General-purpose counter 1 counts down when this pin is at a logic low and counts up at a logic high. You can disable this input so that software can control the up-down functionality and leave

the DIO7 pin free for general use. Figure 4-35 shows the timing requirements for the GATE and SOURCE input signals and the timing specifications for the OUT output signals of the DAQCard-6062E.

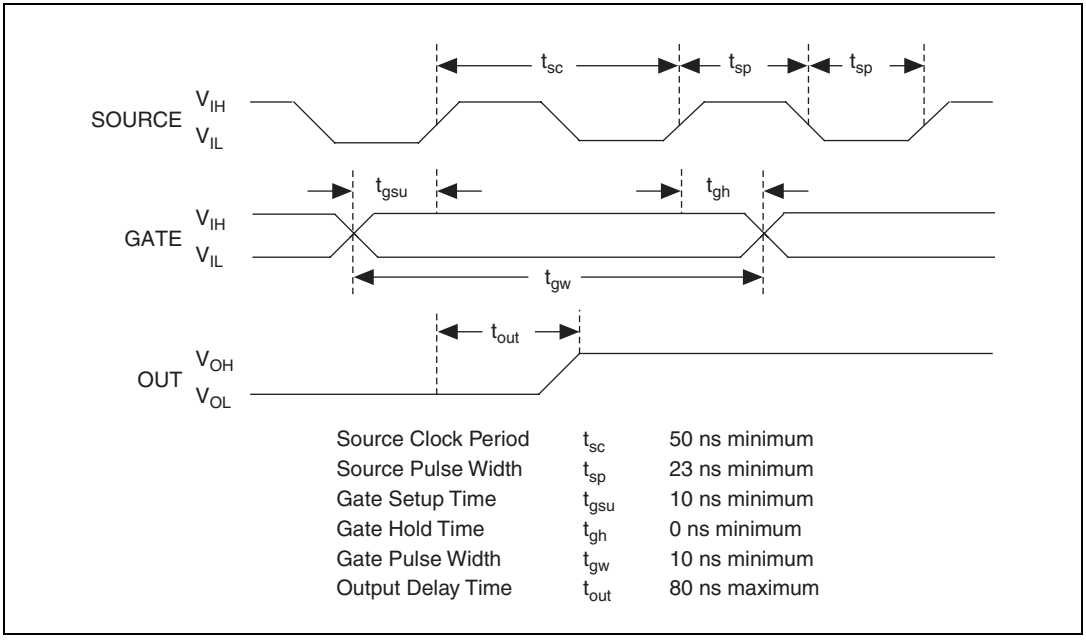


Figure 4-35. GPCTR Timing Summary

The GATE and OUT signal transitions shown in Figure 4-35 are referenced to the rising edge of the SOURCE signal. This timing diagram assumes that the counters are programmed to count rising edges. If the counter is programmed to count falling edges, the source signal is inverted and referenced to the falling edge of the source signal in Figure 4-35.

The GATE input timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated signals on the DAQCard-6062E. Figure 4-35 shows the GATE signal referenced to the rising edge of a source signal. The gate must be valid (either high or low) for at least 10 ns before the rising or falling edge of a source signal for the gate to take effect at that source edge, as shown by t_{gsu} and t_{gh} in Figure 4-35. The gate signal is not required to be held after the active edge of the source signal.

If an internal timebase clock is used, the gate signal cannot be synchronized with the clock. In this case, gates applied close to a source edge take effect either on that source edge or on the next one. This arrangement results in an uncertainty of one source clock period with respect to unsynchronized gating sources.

The OUT output timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated clock signals on the DAQCard-6062E. Figure 4-35 shows the OUT signal referenced to the rising edge of a source signal. Any OUT signal state changes occur within 80 ns after the rising or falling edge of the source signal.

FREQ_OUT Signal

This signal is available only as an output on the FREQ_OUT pin. The FREQ_OUT signal is the output of the DAQCard-6062E frequency generator. The frequency generator is a 4-bit counter that can divide its input clock by the numbers 1 through 16. The input clock of the frequency generator is software-selectable from the internal 10 MHz and 100 kHz timebases. The output polarity is software selectable. This signal is set to high-impedance at startup.

Field Wiring Considerations

Environmental noise can seriously affect the accuracy of measurements made with the DAQCard-6062E if you do not take proper care when running signal wires between signal sources and the DAQCard-6062E. The following recommendations apply mainly to AI signal routing to the DAQCard-6062E although they also apply to signal routing in general.

You can minimize noise pickup and maximize measurement accuracy by taking the following precautions:

- Use differential AI connections to reject common-mode noise.
- Use individually shielded, twisted-pair wires to connect AI signals to the DAQCard-6062E. With this type of wire, the signals attached to the CH+ and CH– inputs are twisted together and then covered with a shield. You then connect this shield only at one point to the signal source ground. This kind of connection is required for signals traveling through areas with large magnetic fields or high electromagnetic interference.
- Route signals to the DAQCard-6062E carefully. Keep cabling away from noise sources. The most common noise source in a

computer-based acquisition system is the video monitor. Separate the monitor from the analog signals as much as possible.

The following recommendations apply for all signal connections to the DAQCard-6062E:

- Separate DAQCard-6062E signal lines from high-current or high-voltage lines. These lines are capable of inducing currents in or voltages on the DAQCard-6062E signal lines if they run in parallel paths at a close distance. To reduce the magnetic coupling between lines, separate them by a reasonable distance if they run in parallel, or run the lines at right angles to each other.
- Do not run signal lines through conduits that also contain power lines.
- Protect signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running them through special metal conduits.

For more information, refer to the NI Developer Zone tutorial, *Field Wiring and Noise Consideration for Analog Signals*, available at `ni.com/zone`.

5

Calibration

This chapter discusses the calibration procedures for the DAQCard-6062E. If you are using NI-DAQ, the software includes calibration functions for performing all the steps in the calibration process.

Calibration refers to the process of minimizing measurement and output voltage errors by making small circuit adjustments. On the DAQCard-6062E, these adjustments take the form of writing values to onboard calibration DACs (CalDACs).

Some form of calibration is required for most applications. Without calibration, the signals and measurements could have very large offset, gain, and linearity errors.

Three levels of calibration are available to you, and these are described in this chapter. The first level is the fastest, easiest, and least accurate, whereas the last level is the slowest, most difficult, and most accurate.

Loading Calibration Constants

The DAQCard-6062E is factory calibrated before shipment at approximately 25 °C to the levels indicated in Appendix A, *Specifications*. The associated calibration constants—the values that were written to the CalDACs to achieve calibration in the factory—are stored in the onboard nonvolatile memory (EEPROM). Because the CalDACs have no memory capability, they do not retain calibration information when the DAQCard-6062E is unpowered. Loading calibration constants refers to the process of loading the CalDACs with the values stored in the EEPROM. NI-DAQ determines when this loading is necessary and does it automatically. If you are not using NI-DAQ, you must load these values.

The EEPROM has a user-modifiable calibration area in addition to the permanent factory calibration area, so you can load the CalDACs with values either from the original factory calibration or from a calibration that you subsequently performed.

This method of calibration is not very accurate because it does not take into account the fact that the DAQCard-6062E measurement and output voltage errors can vary with time and temperature. It is better to self-calibrate when the DAQCard-6062E is installed in the environment in which it will be used.

Self-Calibration

The DAQCard-6062E can measure and correct for almost all calibration-related errors without any external signal connections. NI-DAQ provides a self-calibration method you can use. This self-calibration process, which generally takes less than a minute, is the preferred method of assuring accuracy in your application. Initiate self-calibration to minimize the effects of any offset, gain, and linearity drifts, particularly those effects due to warmup.

Immediately after self-calibration, the only significant residual calibration error could be gain error due to time or temperature drift of the onboard voltage reference. This error is addressed by external calibration, which is discussed in the following section. If you are interested primarily in relative measurements, you can ignore a small amount of gain error, and self-calibration should be sufficient.

External Calibration

The DAQCard-6062E has an onboard calibration reference to ensure the accuracy of self-calibration. These specifications are listed in Appendix A, *Specifications*. The reference voltage is measured at the factory and stored in the EEPROM for subsequent self-calibrations. This voltage is stable enough for most applications, but if you are using the DAQCard-6062E at an extreme temperature, or if the onboard reference has not been measured for a year or more, you may wish to externally calibrate the DAQCard-6062E.

An external calibration refers to calibrating the DAQCard-6062E with a known external reference rather than relying on the onboard reference. Redetermining the value of the onboard reference is part of this process, and you can save the results in the EEPROM so that you should not have to perform an external calibration often. You can externally calibrate the DAQCard-6062E by calling the NI-DAQ calibration function.

To externally calibrate the DAQCard-6062E, use a very accurate external reference. The reference should be several times more accurate than the DAQCard-6062E itself. For example, to calibrate the 12-bit DAQCard-6062E, the external reference should be at least ±0.005% (±50 ppm) accurate.

For a detailed calibration procedure for the DAQCard-6062E, refer to the *E Series Calibration Procedure* by clicking **Manual Calibration Procedures** at `ni.com/calibration`.

Other Considerations

The CalDACs adjust the gain error of each AO channel by adjusting the value of the reference voltage supplied to that channel. This calibration mechanism is designed to work only with the internal 10 V reference. Thus, in general, it is not possible to calibrate the AO gain error when using an external reference. In this case, it is advisable to account for the nominal gain error of the AO channel either in software ow with external hardware. Refer to Appendix A, *Specifications*, for AO gain error information.

A

Specifications

This appendix lists the specifications of the DAQCard-6062E. These specifications are typical at 25 °C unless otherwise noted.

Analog Input

Input Characteristics

Number of channels ..... 16 single-ended,
16 pseudo-differential, or
8 differential (software-selectable on a per channel basis)

Type of ADC..... Successive approximation

Resolution ..... 12 bits, 1 in 4,096

Max sampling rate..... 500 kS/s

Input signal ranges

Board Gain (Software Selectable)	Board Range (Software Selectable)	
	Bipolar	Unipolar
0.5	±10 V	—
1	±5 V	0 to 10 V
2	±2.5 V	0 to 5 V
5	±1	0 to 2 V
10	±500 mV	0 to 1 V
20	±250 mV	0 to 500 mV
50	±100 mV	0 to 200 mV
100	±50 mV	0 to 100 mV

Input coupling.....DC

Max working voltage
(signal + common mode).....Each input should remain within ±11 V of ground

Overvoltage protection .....±25 V powered on, ±15 V powered off

Inputs protected .....ACH<0..15>, AISENSE

FIFO buffer size.....8,192 samples

Data transfers.....Interrupts, programmed I/O

Configuration memory size .....512 words

Transfer Characteristics

Relative accuracy .....±0.5 LSB typ dithered, ±1.5 LSB max undithered

DNL.....–0.9, +1.5 LSB max

No missing codes.....12 bits, guaranteed

Offset error

Pregain error after calibration.....±16 µV max

Pregain error before calibration.....±4 mV max

Postgain error after calibration .....±1 mV max

Postgain error before calibration .....±265 mV max

Gain error (relative to calibration reference)

After calibration (gain = 1).....±0.02% of reading max

Before calibration .....±2.5% of reading max

Gain ≠ 1 with gain error adjusted to 0 at gain = 1 .....±0.02% of reading max

Amplifier Characteristics

Input impedance

Normal powered on ..... 100 GΩ in parallel with 100 pF

Powered off..... 820 Ω min

Overload..... 820 Ω min

Input bias current ..... ±200 pA

Input offset current..... ±100 pA

CMRR (all input ranges, DC to 60 Hz)

Gain ≤ 1 ..... 85 dB

Gain = 2 ..... 95 dB

Gain ≥ 5 ..... 100 dB

Dynamic Characteristics

Bandwidth

Small signal (–3 dB) ..... 1.3 MHz

Large signal (1% THD) ..... 300 kHz

Settling time for full-scale step

Gain	Accuracy[1]	
	±0.012% (±0.5 LSB)	**±0.024% (±1 LSB)**
0.5	2.5 µs typ, 4 µs max	3 µs max

[1]Accuracy values valid for source impedances < 1 kΩ. Refer to the *Multiple Channel Scanning Considerations* section of Chapter 3, *Hardware Overview*, for more information.

System noise in LSB_{rms}, not including quantization

Gain	Noise, Dither Off	Noise, Dither On
0.5 to 10	0.45	0.70
20	0.50	0.75

Gain	Noise, Dither Off	Noise, Dither On
50	0.65	0.8
100	0.9	1.0

Crosstalk (DC to 100 kHz) .....–75 dB (adjacent channels), –90 dB (all other channels), DC to 100 kHz

Stability

Offset temperature coefficient

Pregain.....±5 µV/°C

Postgain .....±240 µV/°C

Gain temperature coefficient .....±20 ppm/°C

Analog Output

Output Characteristics

Number of channels.....2 voltage

Resolution.....12 bits, 1 in 4,096

Max update rate

FIFO Mode		Non-FIFO Mode	
Internally Timed	**Externally Timed**	**1 Channel**	**2 Channels**
850 kS/s	850 kS/s	800 kS/s, system dependent	400 kS/s, system dependent

Type of DAC .....Double-buffered, multiplying

FIFO buffer size.....2,048 samples

Data transfers.....interrupts, programmed I/O

Transfer Characteristics

Relative accuracy (INL)

- After calibration ..... ±0.5 LSB typ, ±1.0 LSB max
- Before calibration ..... ±4 LSB max

DNL

- After calibration ..... ±0.5 LSB typ, ±1.0 LSB max
- Before calibration ..... ±3 LSB max

Monotonicity ..... 12 bits, guaranteed after calibration

Offset error

- After calibration ..... ±1.0 mV max
- Before calibration ..... ±200 mV max

Gain error (relative to internal reference)

- After calibration ..... ±0.01% of output max
- Before calibration ..... ±0.7% of output max

Gain error (relative to external reference) ..... ±0.5% of output max, not adjustable

Voltage Output

Ranges ..... ±10 V, ±EXTREF, (software-selectable)

Output coupling ..... DC

Output impedance ..... 0.1 Ω max

Current drive ..... ±5 mA max

Protection ..... Short-circuit to ground

Power-on state ..... 0 V (± 200 mV)

External reference input

- Range ..... ±11 V
- Overvoltage protection ..... ±25 V powered on, ±15 V powered off

Input impedance .....10 kΩ
Bandwidth (–3 dB) .....50 kHz

Dynamic Characteristics

Settling time for full-scale step.....3 µs to ±0.5 LSB accuracy

Slew rate .....20 V/µs

Noise.....200 μV_{rms}, DC to 1 MHz

Glitch energy (at midscale transition)
Magnitude
Reglitching disabled.....±20 mV
Reglitching enabled.....±4 mV
Duration.....1.5 µs

Stability

Offset temperature coefficient.....±50 µV/°C

Gain temperature coefficient
Internal reference.....±25 ppm/°C
External reference.....±25 ppm/°C

Digital I/O

Number of channels.....8 input/output

Compatibility .....TTL/CMOS

Digital logic levels

Level	Min	Max
Input low voltage	0 V	0.8 V
Input high voltage	2 V	5 V
Input low current (V_{in} = 0 V)	—	–320 µA
Input high current (V_{in} = 5 V)	—	10 µA
Output low voltage (I_{OL} = 24 mA)	—	0.4 V
Output high voltage (I_{OH} = 13 mA)	4.35 V	—

Power-on state ..... High-impedance

Data transfers ..... Programmed I/O

Max transfer rate ..... 50 kwords/s, system dependent

Constant sustainable rate ..... 1 to 10 kwords/s, typ

Timing I/O

Number of channels ..... 2 up/down counter/timers, 1 frequency scaler

Resolution

- Counter/timers ..... 24 bits
- Frequency scalers ..... 4 bits

Compatibility ..... TTL/CMOS

Base clocks available

- Counter/timers ..... 20 MHz, 100 kHz
- Frequency scalers ..... 10 MHz, 100 kHz

Base clock accuracy ..... ±0.01%

Max source frequency ..... 20 MHz

Min source pulse duration ..... 10 ns in edge-detection mode

Min gate pulse duration ..... 10 ns in edge-detection mode

Data transfers ..... Interrupts, programmed I/O

Triggers

Analog Trigger

Source ..... ACH<0..15>, external trigger (PFI0/TRIG1)

Level ..... ± full-scale, internal; ±10 V, external

Slope ..... Positive or negative (software-selectable)

Resolution.....8 bits, 1 in 256

Hysteresis.....Programmable

Bandwidth (–3 dB).....500 kHz internal,
2.5 MHz external

External input (PFI0/TRIG1)

- Impedance.....12 kΩ
- Coupling.....DC
- Protection.....±35 V powered off,
–0.5 to V_{CC} when configured as a digital signal,
±35 V when configured as an analog trigger signal or disabled

Digital Trigger

Compatibility.....TTL

Response.....Rising or falling edge

Pulse width.....10 ns min

Calibration

Recommended warm-up time.....15 min

Calibration interval.....1 year

External calibration reference.....>6 and <9.999 V

Onboard calibration reference

- Level.....5.000 V (±2.5 mV)
(actual value stored in EEPROM)
- Temperature coefficient.....±5 ppm/°C max
- Long-term stability.....±15 ppm/$\sqrt{1{,}000\ \text{h}}$

Power Requirement (from PCMCIA I/O Channel)

+5 VDC (±5%)..... 330 mA typ in operational mode, 450 mA max in operational mode, 100 mA in power-down mode

Power available at I/O connector..... +4.65 to +5.25 V at 250 mA

Notes These power usage figures do not include the power used by external devices that are connected to the fused supply present on the I/O connector.

Under ordinary operation, the DAQCard has a current requirement of 320–350 mA; but if the analog inputs being sampled are overdriven at high gains, or if the analog inputs are left floating when the DAQCard is not in use, or if the analog outputs are loaded down, the current may increase to 450 mA.

Physical

PC card type..... Type II

I/O connector..... 68-position VHDCI female connector

Environmental

Operating temperature..... 0 to 50 °C, internal device temperature as measured by internal termperature sensor

Storage temperature..... –20 to 70 °C

Humidity..... 5 to 90% RH, noncondensing

Maximum altitude..... 2,000 meters

Pollution degree (indoor use only)..... 2

Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Channel-to-earth..... 42 V, Installation Category II

Channel-to-channel..... 42 V, Installation Category II

Safety

The DAQCard-6062E meets the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use:

- EN 61010-1:1993/A2:1995, IEC 61010-1:1990/A2:1995
- UL 3101-1:1993, UL 3111-1:1994, UL 3121:1998
- CAN/CSA c22.2 no. 1010.1:1992/A2:1997

Electromagnetic Compatibility

CE, C-Tick, and FCC Part 15 (Class A) Compliant

Electrical emissions .....EN 55011 Class A at 10 m
FCC Part 15A above 1 GHz

Electrical immunity .....Evaluated to EN 61326:1997/
A1:1998, Table 1

Note For full EMC compliance, you must operate this device with shielded cabling. In addition, all covers and filler panels must be installed. Refer to the DoC for this product for any additional regulatory compliance information. To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by your product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.

B

Optional Cable Connector Descriptions

This appendix describes the connectors on the optional cables for the DAQCard-6062E.

Figure B-1 shows the pin assignments for the 68-pin E Series connector. This connector is available when you use the SHC68-68-EP cable assembly.

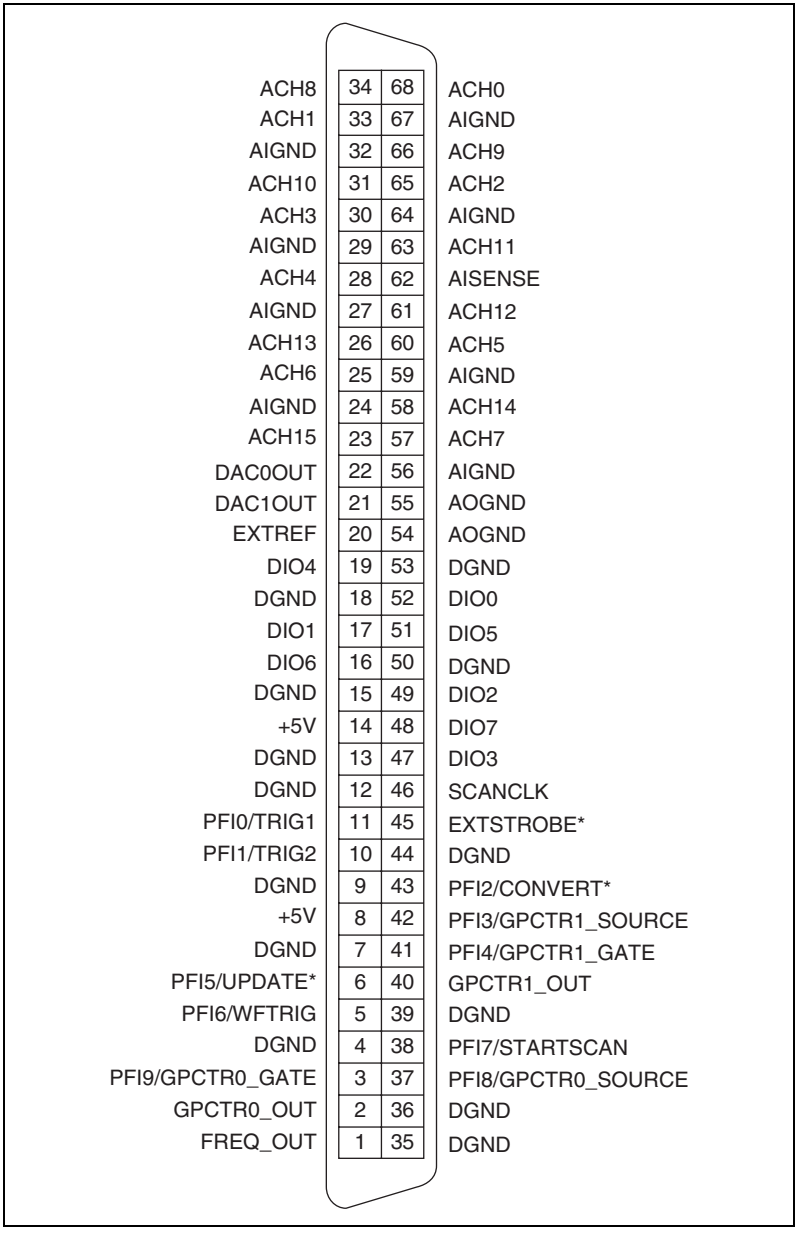


Figure B-1. 68-Pin E Series Connector Pin Assignments

Figure B-2 shows the pin assignments for the 50-pin E Series connector. This connector is available when you use the SHC68-68-EP cable assembly with the 68M-50F.

AIGND	1	2	AIGND
ACH0	3	4	ACH8
ACH1	5	6	ACH9
ACH2	7	8	ACH10
ACH3	9	10	ACH11
ACH4	11	12	ACH12
ACH5	13	14	ACH13
ACH6	15	16	ACH14
ACH7	17	18	ACH15
AISENSE	19	20	DAC0OUT
DAC1OUT	21	22	EXTREF
AOGND	23	24	DGND
DIO0	25	26	DIO4
DIO1	27	28	DIO5
DIO2	29	30	DIO6
DIO3	31	32	DIO7
DGND	33	34	+5V
+5V	35	36	SCANCLK
EXTSTROBE*	37	38	PFI0/TRIG1
PFI1/TRIG2	39	40	PFI2/CONVERT*
PFI3/GPCTR1_SOURCE	41	42	PFI4/GPCTR1_GATE
GPCTR1_OUT	43	44	PFI5/UPDATE*
PFI6/WFTRIG	45	46	PFI7/STARTSCAN
PFI8/GPCTR0_SOURCE	47	48	PFI9/GPCTR0_GATE
GPCTR0_OUT	49	50	FREQ_OUT

Figure B-2. 50-Pin E Series Connector Pin Assignments

C

Common Questions

This appendix contains a list of commonly asked questions and their answers relating to usage and special features of the DAQCard-6062E.

General Information

What is the DAQ-STC?

The DAQ-STC is the system timing control ASIC (application-specific integrated circuit) designed by National Instruments and is the backbone of the DAQCard-6062E. The DAQ-STC contains seven 24-bit counters and three 16-bit counters. The counters are divided into three groups:

- AI—two 24-bit, two 16-bit counters
- AO—three 24-bit, one 16-bit counters
- General-purpose counter/timer functions—two 24-bit counters

You can independently configure the groups with timing resolutions of 50 ns or 10 µs. With the DAQ-STC, you can interconnect a wide variety of internal timing signals to other internal blocks. The interconnection scheme is quite flexible and completely software configurable. New capabilities, such as buffered pulse generation, equivalent time sampling, and seamlessly changing the sampling rate, are possible.

What type of 5 V protection does the DAQCard-6062E have?

The DAQCard-6062E has 5 V lines equipped with a self-resetting 250 mA fuse.

How do I use the DAQCard-6062E with the C API in NI-DAQ?

The *NI-DAQ User Manual for PC Compatibles* contains example code and describes the general programming flow when using the NI-DAQ C API. For a list of functions that support the DAQCard-6062E, refer to the *NI-DAQ Function Reference Help.*

Refer to ni.com/manuals for the *NI-DAQ User Manual for PC Compatibles*, and refer to ni.com/downloads to download the version of NI-DAQ that your application requires. To access the NI-DAQ Function Reference Help, select **Start»Programs»National Instruments» NI-DAQ»NI-DAQ Help**.

Installing and Configuring

Which National Instruments documentation should I read first to get started using DAQ software?

The *DAQ Quick Start Guide* and the NI-DAQ or ADE release notes documentation are good places to start.

What version of NI-DAQ must I have to program the DAQCard-6062E?

You must have version 6.7 or later.

What is the best way to test my DAQCard without having to program the DAQCard?

If you are using Windows, MAX has a Test Panel option that is available by selecting **Devices and Interfaces** and then selecting the device. The Test Panels are excellent tools for performing simple functional tests of the device, such as AI, DIO, and counter/timer tests.

Analog Input and Output

I'm using the DAQCard in DIFF mode, and I have connected a DIFF input signal, but the readings are random and drift rapidly. What's wrong?

Check the ground-reference connections. The signal may be referenced to a level that is considered *floating* with reference to the DAQCard ground reference. Even if you are in differential mode, the signal *must* still be referenced to the same ground level as the DAQCard reference. There are various methods of achieving the same ground level while maintaining a high common-mode rejection ratio (CMRR). These methods are outlined in Chapter 4, *Signal Connections*.

Can I sample across a number of channels on a DAQCard-6062E while each channel is being sampled at a different rate?

NI-DAQ features a function called `SCAN_Sequence_Setup`, which allows for multirate scanning of the AI channels. Refer to the *NI-DAQ Function Reference Online Help* for more details.

Can I programmatically enable channels on the DAQCard-6062E to acquire in different modes? For example, can I configure ACH 0 in DIFF input mode and ACH1 in RSE input mode?

Channels on the DAQCard-6062E can be enabled to acquire in different modes, but different pairs of channels are used in different modes. In the example configuration given above, ACH0 and ACH8 are configured in DIFF mode and ACH1 and AIGND are configured in RSE mode. In this configuration, ACH8 is not used in a single-ended configuration. To enable multiple mode scanning in LabVIEW, use the coupling and input configuration cluster input of the AI Config VI. This input has a one-to-one correspondence with the channel array input of the AI Config VI. You must list all channels either individually or in groups of channels with the same input configuration. For example, if you want ACH0 to be differential, and ACH1 and ACH2 to be RSE, Figure C-1 demonstrates how to program this configuration in LabVIEW.

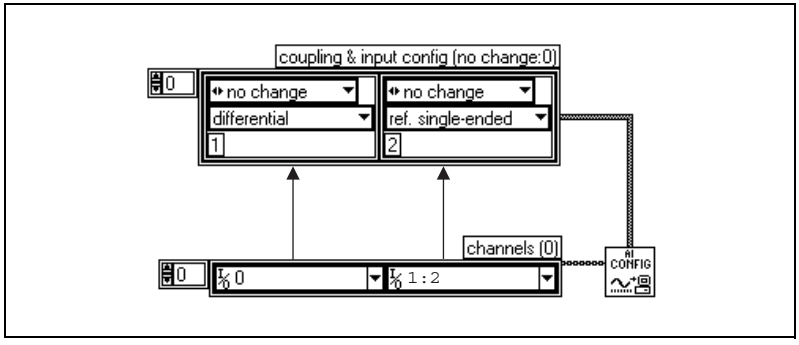


Figure C-1. Configuring Channels for Different Acquisition Modes in LabVIEW

To enable multiple mode scanning using NI-DAQ functions, call the `AI_Configure` function for each channel.

I am seeing crosstalk or ghost voltages when sampling multiple channels. What does this mean?

You maybe experiencing a phenomenon called *charge injection*, which occurs when you sample a series of high-output impedance sources with a multiplexer. Multiplexers contain switches, usually made of switched capacitors. When a channel, for example ACH0, is selected in a multiplexer, those capacitors accumulate charge. When the next channel, for example ACH1, is selected, the accumulated current (i.e., charge) leaks backward through that channel. If the output impedance of the source connected to ACH1 is high enough, the resulting reading can somewhat reflect the voltage trends in ACH0. To circumvent this problem, you must use a voltage follower that has operational amplifiers (op-amps) with unity gain for each high-impedance source before connecting to the DAQ device. Otherwise, you must decrease the rate at which each channel is sampled.

Another common cause of channel crosstalk is due to sampling among multiple channels at various gains. In this situation, the settling times may increase. For more information on charge injection and sampling channels at different gains, refer to the *Multiple Channel Scanning Considerations* section of Chapter 3, *Hardware Overview*.

I'm using the DACs to generate a waveform, but I discovered with a digital oscilloscope that there are glitches on the output signal. Is this normal?

When it switches from one voltage to another, any DAC produces glitches due to released charges. The largest glitches occur when the most significant bit (MSB) of the D/A code switches. A lowpass deglitching filter can help to remove some of these glitches, depending on the frequency and nature of the output signal. The DAQCard-6062E has built-in reglitchers, which can be software-enabled, on its AO channels.

Can I synchronize a one-channel AI data acquisition with a one-channel AO waveform generation on the DAQCard-6062E?

Yes. One way to synchronize the channels is to use the waveform generation timing pulses to control the AI data acquisition. To do this, follow steps 1 through 4, in addition to the usual steps for data acquisition and waveform generation configuration.

1. Enable the PFI5 line for output, as follows:
   - If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_PFI_5, ND_OUT_UPDATE, ND_HIGH_TO_LOW).`

- If you are using LabVIEW, invoke Route Signal VI with signal name set to PFI5 and signal source set to AO Update.

2. Set up data acquisition timing so that the timing signal for A/D conversion comes from PFI5, as follows:
   - If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_IN_CONVERT, ND_PFI_5, ND_HIGH_TO_LOW).`
   - If you are using LabVIEW, invoke AI_Clock_Config_VI with clock source code set to PFI pin, high to low, and clock source string set to 5.
3. Initiate AI data acquisition, which will start only when the AO waveform generation starts.
4. Initiate AO waveform generation.

How can I use the STARTSCAN and CONVERT* signals on the DAQCard-6062E to sample the AI channel(s)?

NI E Series devices use the STARTSCAN and CONVERT* signals to perform interval sampling. As Figure C-2 shows, STARTSCAN controls the scan interval, which is determined by the following equality:

$$\frac{1}{scan\ interval} = scan\ rate$$

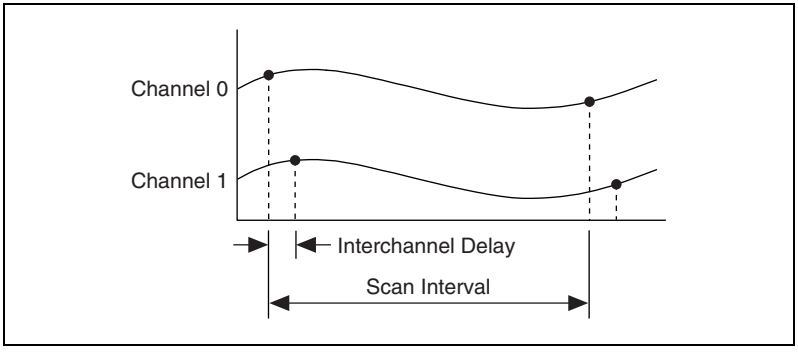


Figure C-2. Interchannel Delay and Scan Interval

CONVERT* controls the interchannel delay, which is determined by the following equality:

$$\frac{1}{interchannel\ delay} = sampling\ rate$$

This method allows multiple channels to be sampled relatively quickly in relationship to the overall scan rate, providing a nearly simultaneous effect with a fixed delay between channels.

Timing and Digital I/O

What types of triggering can be implemented in hardware on my DAQCard-6062E?

Digital and analog triggering are hardware supported on the DAQCard-6062E.

Will the counter/timer applications that I wrote previously work with the DAQ-STC?

If you are using the NI-DAQ with LabVIEW, some of your applications drawn using the CTR VIs will still run. However, there are many differences in the counters between the DAQCard-6062E and other devices—the counter numbers are different; timebase selections are different; and the DAQ-STC counters are 24-bit counters (unlike the 16-bit counters on devices without the DAQ-STC).

If you are using the NI-DAQ language interface, such as LabWindows/CVI, the counter/time applications that you wrote previously will not work with the DAQ-STC. You must use the GPCTR functions; ICTR and CTR functions will not work with the DAQ-STC. The GPCTR functions have the same capabilities as the ICTR and CTR functions, plus more, but you must rewrite the application with the GPCTR function calls.

I'm using one of the general-purpose counter/timers on my DAQCard-6062E, but I do not see the counter/timer output on the I/O connector. What am I doing wrong?

If you are using the NI-DAQ language interface or LabWindows/CVI, you must configure the output line to output the signal to the I/O connector. Use the `Select_Signal` call in NI-DAQ to configure the output line. By default, all timing I/O lines except EXTSTROBE* are high-impedance.

What are the PFIs, and how do I configure these lines?

PFIs are Programmable Function Inputs. These lines serve as connections to virtually all internal timing signals.

If you use NI-DAQ or Measurement Studio, use the `Select_Signal` function to route internal signals to the I/O connector, route external signals to internal timing sources, or tie internal timing signals together.

If you are using NI-DAQ with LabVIEW and you want to connect external signal sources to the PFI lines, you can use AI Clock Config, AI Trigger Config, AO Clock Config, AO Trigger and Gate Config, and Counter Set Attribute advanced level VIs to indicate which function the connected signal will serve. Use the Route Signal VI to enable the PFI lines to output internal signals.

Caution If you enable a PFI line for output, do *not* connect any external signal source to it; if you do, you can damage the DAQCard, the computer, and the connected equipment.

Table C-1 corresponds the hardware signal names to the software signal names in LabVIEW and NI-DAQ.

Table C-1. Signal Name Equivalencies

Hardware Signal Name	LabVIEW Route Signal	NI-DAQ Select_Signal
TRIG1	AI Start Trigger	ND_IN_START_TRIGGER
TRIG2	AI Stop Trigger	ND_IN_STOP_TRIGGER
STARTSCAN	AI Scan Start	ND_IN_SCAN_START
SISOURCE	—	ND_IN_SCAN_CLOCK_TIMEBASE
CONVERT*	AI Convert	ND_IN_CONVERT
AIGATE	—	ND_IN_EXTERNAL_GATE
WFTRIG	AO Start Trigger	ND_OUT_START_TRIGGER
UPDATE*	AO Update	ND_OUT_UPDATE
UISOURCE	—	ND_OUT_UPDATE_CLOCK_TIMEBASE
AOGATE	—	ND_OUT_EXTERNAL_GATE

What are the power-on states of the PFI and DIO lines on the I/O connector?

At system power-on and reset, both the PFI and DIO lines are set to high-impedance by the hardware. This setting means that the device circuitry is not actively driving the output either high or low. However, these lines may have pull-up or pull-down resistors connected to them as shown in Tables 4-2 and 4-3. These resistors weakly pull the output to either a logic high or logic low state. For example, DIO(0) will be in the high impedance state after power on, and Table 4-2 shows that there is a 50 kΩ pull-up resistor. This pull-up resistor will set the DIO(0) pin to a logic high when the output is in a high-impedance state.

D

Technical Support and Professional Services

Visit the following sections of the NI Web site at ni.com for technical support and professional services:

- **Support**—Online technical support resources include the following:
  - **Self-Help Resources**—For immediate answers and solutions, visit our extensive library of technical support resources available in English, Japanese, and Spanish at ni.com/support. These resources are available for most products at no cost to registered users and include software drivers and updates, a KnowledgeBase, product manuals, step-by-step troubleshooting wizards, hardware schematics and conformity documentation, example code, tutorials and application notes, instrument drivers, discussion forums, a measurement glossary, and so on.
  - **Assisted Support Options**—Contact NI engineers and other measurement and automation professionals by visiting ni.com/ask. Our online system helps you define your question and connects you to the experts by phone, discussion forum, or email.
- **Training**—Visit ni.com/custed for self-paced tutorials, videos, and interactive CDs. You also can register for instructor-led, hands-on courses at locations around the world.
- **System Integration**—If you have time constraints, limited in-house technical resources, or other project challenges, NI Alliance Program members can help. To learn more, call your local NI office or visit ni.com/alliance.

If you searched ni.com and could not find the answers you need, contact your local office or NI corporate headquarters. Phone numbers for our worldwide offices are listed at the front of this manual. You also can visit the Worldwide Offices section of ni.com/niglobal to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

Glossary

Prefix	Meanings	Value
p-	pico-	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{9}

Symbols

°	degrees
–	negative of, or minus
Ω	ohms
/	per
%	percent
±	plus or minus
+	positive of, or plus
$\sqrt{\ }$	square root of
+5V	+5 VDC source signal

A

A	amperes
A/D	analog-to-digital
AC	alternating current
ACH	analog input channel signal
ADC	analog-to-digital converter—an electronic device, often an integrated circuit, that converts an analog voltage to a digital number
ADE	application development environment
ADIO	analog/digital input/output
AI	analog input
AIGATE	analog input gate signal
AIGND	analog input ground signal
AISENSE	analog input sense signal
AO	analog output
AOGND	analog output ground signal
ASIC	application-specific integrated circuit

B

BC	buffer counter
BIOS	basic input/output system or built-in operating system

C

C	Celsius
CalDAC	calibration DAC
CH	channel

channel rate	reciprocal of the interchannel delay
CIS	Card Information Structure
cm	centimeter
CMOS	complementary metal-oxide semiconductor
CMRR	common-mode rejection ratio
CONVERT*	convert signal
CTR	counter

D

D/A	digital-to-analog
DAC	digital-to-analog converter—an electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current
DAC0OUT	analog channel 0 output signal
DAC1OUT	analog channel 1 output signal
DAQ	data acquisition—a system that uses the computer to collect, receive, and generate electrical signals
DAQCard	data acquisition card
DAQ-STC	National Instruments data acquisition system timing controller
dB	decibel—the unit for expressing a logarithmic measure of the ratio of two signal levels: dB = 20log10 V1/V2, for signals in volts
DC	direct current
DGND	digital ground signal
DIFF	differential
DIO	digital input/output

DMA	direct memory access—a method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.
DNL	differential nonlinearity
DO	digital output
DoC	Declaration of Conformity
DOC	Department of Communications
DOS	disk operating system

E

EEPROM	electrically erasable programmable read-only memory
EISA	Extended Industry Standard Architecture
EPROM	erasable programmable read-only memory
EXTREF	external reference signal
EXTSTROBE	external strobe signal

F

F	farads
FCC	Federal Communications Commission

FIFO	first-in first-out memory buffer—FIFOs are often used on DAQ devices to temporarily store incoming or outgoing data until that data can be read or written. For example, an analog input FIFO stores the results of A/D conversions until the data can be read into system memory. Programming the DMA controller and servicing interrupts can take several milliseconds in some cases. During this time, data accumulates in the FIFO for future retrieval. With a larger FIFO, longer latencies can be tolerated. In the case of analog output, a FIFO permits faster update rates, because the waveform data can be stored in the FIFO ahead of time. This again reduces the effect of latencies associated with getting the data from system memory to the DAQ device.
floating signal sources	signal sources with voltage signals that are not connected to an absolute reference or system ground. Also called nonreferenced signal sources. Some common example of floating signal sources are batteries, transformers, or thermocouples.
FREQ_OUT	frequency output signal
ft	feet

G

gain	the factor by which a signal is amplified, often expressed in dB
GATE	gate signal
GPCTR	general purpose counter
GPCTR0_GATE	general purpose counter 0 gate signal
GPCTR0_OUT	general purpose counter 0 output signal
GPCTR0_SOURCE	general purpose counter 0 clock source signal
GPTR0_UP_DOWN	general purpose counter 0 up down signal
GPCTR1_GATE	general purpose counter 1 gate signal
GPCTR1_OUT	general purpose counter 1 output signal
GPCTR1_SOURCE	general purpose counter 1 clock source signal

GPTR1_UP_DOWN	general purpose counter 1 up down signal
grounded signal sources	*See* referenced signal sources.

H

h	hour
hex	hexadecimal
hysteresis	lag between making a change and the effect of the change
Hz	hertz

I

I/O	input/output—the transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces
ICTR	input counter
I_{OH}	current, output high
I_{OL}	current, output low
INL	relative accuracy
interchannel delay	amount of time that passes between sampling consecutive channels. The interchannel delay must be short enough to alloy sampling of all the channels in the channel list, within the scan interval. The greater the interchannel delay, the more time the PGIA is allowed to settle before the next channel is sampled. The interchannel delay is regulated by the CONVERT* signal.
IRQ	interrupt request signal
ISA	Industry Standard Architecture

L

LED	light emitting diode
LSB	least significant bit

M

m	meter
MB	megabytes of memory
MIO	multifunction I/O
MSB	most significant bit

N

NC	not connected internally
NI	National Instruments
NI-DAQ	NI driver software for DAQ hardware
NRSE	nonreferenced single-ended

O

OUT	output signal

P

PC	personal computer
PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations; it offers a theoretical maximum transfer rate of 132 MB/s.
PCMCIA	Personal Computer Memory Card Association

PFI	Programmable Function Input
PFI0/TRIG1	PFI0/trigger 1
PFI1/TRIG2	PFI1/trigger 2
PFI2/CONVERT*	PFI2/convert
PFI3/GPCTR1_SOURCE	PFI3/general purpose counter 1 source
PFI4/GPCTR1_GATE	PFI4/general purpose counter 1 gate
PFI5/UPDATE*	PFI5/update
PFI6/WFTRIG	PFI6/waveform trigger
PFI7/STARTSCAN	PFI7/start of scan
PFI8/GPCTR0_SOURCE	PFI8/general purpose counter 0 source
PFI9/GPCTR0_GATE	PFI9/general purpose counter 0 gate
PGIA	Programmable Gain Instrumentation Amplifier
ppm	parts per million
precision	measure of the stability of an instrument and its capability to give the same measurement over and over again for the same input signal
pu	pull-up
PWRDOWN	power down signal

R

RAM	random access memory
range	the maximum and minimum parameters between which a sensor, instrument, or device operates with a specified set of characteristics
REF	reference
referenced signal sources	signal sources with voltage signals that are referenced to a system ground, such as the earth or a building ground. Also called grounded signal sources.

reglitch	to modify the glitches in a signal in order to make them less disruptive
rms	root mean square
RSE	referenced single-ended
RTD	resistive temperature detector—a metallic probe that measures temperature based upon its coefficient of resistivity
RTSI	real-time system integration bus—the National Instruments timing bus that connects DAQ boards directly, by means of connectors on top of the boards, for precise synchronization of functions

S

s	seconds
S	samples
SC	scan counter
SCANCLK	scan clock signal
scan interval	controls how often a scan is initialized; is regulated by the STARTSCAN signal
scan rate	reciprocal of the scan interval
SCXI	Signal Conditioning eXtensions for Instrumentation—the National Instruments product line for conditioning low-level signals within an external chassis near sensors so only high-level signals are sent to DAQ boards in the noisy computer environment
SE	single-ended—a term used to describe an analog input that is measured with respect to a common ground
settling time	time required for an amplifier, relays, or other circuits to reach a stable mode of operation
SI	scan interval counter

SI2	sample interval counter
SISOURCE	SI counter clock signal
STARTSCAN	start scan signal

T

TC	terminal count signal
t_d	delay time
t_{gh}	gate hold time
t_{gsu}	gate setup time
t_{gw}	gate pulse width
THD	total harmonic distortion—the ratio of the total rms signal due to harmonic distortion to the overall rms signal, in dB or percent
TIO	timing I/O
t_{off}	an offset (delayed) pulse; the offset is *t* nanoseconds from the falling edge of the CONVERT* signal
t_{out}	output delay time
t_p	pulse period
TRIG	trigger signal
t_{sc}	source clock period
t_{sp}	source pulse width
TTL	transistor-transistor logic
t_w	pulse width

U

UI	update interval
UISOURCE	update interval counter clock signal
UPDATE*	update signal

V

V	volts
V_{CC}	positive voltage supply
VDC	volts direct current
VI	virtual instrument—(1) a combination of hardware and/or software elements, typically used with a PC, that has the functionality of a classic stand-alone instrument (2) a LabVIEW software module (VI), which consists of a front panel user interface and a block diagram program
V_{IH}	volts, input high
V_{IL}	volts, input low
V_{in}	volts in
V_o	volts, output
V_{OH}	volts, output high
V_{OL}	volts, output low
V_{ref}	reference voltage

W

W	watts
waveform	multiple voltage readings taken at a specific sampling rate
WFTRIG	waveform generation trigger signal

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